ELECTRIC FIELD EMISSIONS OF FPGA CHIP BASED ON GIGAHERTZ TRANSVERSE ELECTROMAGNETIC CELL MODELING AND MEASUREMENTS

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DEDICATION

To my beloved mother and family.

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ABSTRACT

Modern integrated circuits (ICs) are significant sources of undesired electromagnetic wave. Therefore, characterization of chip-level emission is essential to comply with EMC tests at the product level. A Gigahertz Transverse Electromagnetic (GTEM) cell is a common test instrument used to measure IC radiated emission and the test cost is relatively low. Regular IC radiated emission measurements using GTEM tend to neglect some significant emission sources. Thus, this research proposed an alternative methodology to perform field measurement of the IC inside the GTEM cell in order to optimize the field measurements. This research study also attempted analysis of the overall GTEM cell performance using transmission line theory. An FPGA chip was adopted as the IC under test because of its flexibility in configuration to any digital circuit. The investigations discovered that the impact of the FPGA board supporting components and interconnection cables can be significantly reduced with appropriate shielding and grounding. The electric field predict a far distance from the FPGA chip was carried out based on the dipole moment technique. In particular, the dipole moment model emphasizing the tiny horizontal and vertical radiation elements inside the FPGA chip as Hertzian antenna and small current loop. Equations to predict the horizontal and vertical electric field were developed based on Hertzian antenna and small current loop which relate the tiny radiation sources to electric and magnetic dipole moments. The prediction was validated with 3-meter field measurements in a semi-anechoic chamber. On top of that, a spiral-like pattern was developed to obtain a correction factor for further improvement of the correlation between prediction and SAC measurement. The results revealed that the correction factor effectively reduced the gap between the prediction and measurement fields and boosted the correlation coefficient by 44%. The difference of peak values also has limited to less than 10dB after correction. These results suggest a promising finding for a future EMI test of ICs with a cheaper GTEM cell.

ABSTRAK

Litar bersepadu (IC) moden adalah sumber penting menyumbang kepada gelombang electromagnet yang tidak diingini. Oleh sebab ini, penyifatan pengeluaran peringkat cip adalah penting untuk mematuhi ujian EMC di peringkat produk. Sel elektromagnetik melintang gigahertz (GTEM) ialah satu alatan yang biasa digunakan untuk mengukur medan IC yang telah dipancarkan dan kos ujian adalah agak murah. Satu ujian mengukur pancaran medan IC biasa yang dilakukan dengan mengapit papan ujian IC di dinding sel GTEM, yang hamper mengabaikan beberapa sumber pengeluaran penting. Oleh itu, kajian ini telah mencadangkan satu keadah alternatif untuk melaksanakan pengukuran medan IC di dalam sel GTEM untuk mengoptimakan pengukuran medan. Kajian manganalisa prestasi keseluruhan sel GTEM menggunakan teori talian penghantaran. Cip FPGA telah dipilih sebagai peranti dalam ujian kerana ia fleksibe ditatarajah dengan sebarang litar berdigit. Penyiasatan menemui bahawa kesan komponen sokongan papan FPGA dan kabel saling sambung boleh dikurangkan melalui perisaian dan pembumian yang sesuai. Sinaran medan elektrik sepadan pada jarak jauh cip FPGA diramal berasaskan teknik momen dwikutub. Khususnya, model momen dwikutub mewakili sumber pancaran cip yang kecil mendatar dan menegak sebagai antena Hertzian dan gelung arus kecil. Persamaan untuk meramal medan elektrik mendatar dan menegak diterbit daripada antena Hertzian dan gelung arus kecil, dimana sumber pancaran ruas kecil dikaitkan dengan momen dwikutub elektrik dan magnetik. Ramalan ini telah disahkan menggunakan ukuran SAC 3 meter. Untuk penambahbaikan, satu corak pusaran dibentukkan untuk membangun satu faktor pembetulan bagi tujuan meningkatkan lolerasi antara ramalan dan ukuran SAC. Keputusan mendedahkan bahawa faktor pembetulan adalah berkesan untuk mengurangkan jarak antara medan ramalan dan ukuran dan meningkatkan pekali kolerasi sebanyak 44%. Perbezaan dalam nilai-nilai puncak selepas pembetulan juga telah diambil kira bawah 10dB. Hasil keputusan ini mencadangkan satu pencarian yang menjanjikan satu ujian EMI IC masa hadapan dengan sel GTEM yang lebih murah.

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LIST OF SYMBOL

Symbol	Description	Unit
E	Electric Field Intensity	V/m
H	Magnetic Field Intensity	A/m
Z	Wave Impedance	Ω
Z_0	Characteristic Impedance	Ω
Z_L	Load Impedance	Ω
Z_S	Source Impedance	Ω
RL	Return Loss	dB
P_r	Reflected Power	W
P_i	Incident Power	W
f_r	Resonant Frequency	Hz
δ	Skin Depth	m
σ	Conductivity	S/m
μ	Relative Permeability	H/m
μ_0	Relative Permeability of Free-Space, $\mu_0 = 4\pi \times 10^{-7}$	H/m
μ_r	Relative Permeability of Material (dimensionless)	
Γ	Reflection Coefficient (dimensionless)	
θ_r	Phase Angle	degree (°)
β	Phase Constant	rad/m
c	Speed of Light in Vacuum	cm/s
V	Voltage	V
V_L	Load voltage	V
V_i	Input voltage	V
F	Electric Force	N
q	Electric Charge	C
W	Work	J
$\hat{I}_D$	Differential-mode Current	A

Symbol	Description	Unit
L	Inductance	H
C	Capacitance	F
$\boldsymbol{E}$	Electric Field Vector	V/m
$\boldsymbol{H}$	Magnetic Field Vector	A/m
a_n	Forward Excitation Coefficient (dimensionless)	
b_n	Backward Excitation Coefficient (dimensionless)	
k_n	Propagation Constant (dimensionless)	
e_n	Normalized Electric Field Component	
h_n	Normalized Magnetic Field Component	
δ_{mn}	Kronecker Delta Function	
J	Current Density	A/cm^2
P	Electric Dipole Moment	C.m
M	Magnetic Dipole Moment	$A.m^2 = J/T$
a	Cell Width	m
g	Septum Height	m
y	Gap Width	m
V_{ij}	GTEM Measured Voltage	dBμV
b_{ij}	GTEM Correspondence Voltage	$V^2 \cdot m^2/\Omega^2$
e_{0y}	Vertical Electric Field Component at Origin	$\sqrt{\Omega}/m$
η_0	Intrinsic Impedance of Free Space, $\eta_0 = 120\pi$	Ω
α	Angle Across Vertical Axis Rotation	degree (°)
φ	Phase of Moments	rad/m
ω	Radian Frequency of Waveform	rad/s

LIST OF ABBREVIATION

Abbreviation	Description
EMC	Electromagnetic Compatibility
EM	Electromagnetic
EMI	Electromagnetic Interference
RFI	Radio Frequency Interference
EMP	Electromagnetic Pulse
IC	Integrated Circuit
I/O	Input / Output
FPGA	Field Programmable Gate Array
NREs	Non-Recurring Expenses
ASIC	Application-Specific Integrated Circuit
SAE	Society of Automotive Engineer
IEC	International Electrotechnical Commission
PCB	Printed Circuit Board
TEM	Transverse Electromagnetic Mode
GTEM	Gigahertz Transverse Electromagnetic Mode
SAC	Semi-Anechoic Chamber
PLD	Programmable Logic Device
CPLD	Complex Programmable Logic Device
CAD	Computer Aided Design
CACA	Computer-Aided Circuit Analysis
MOS	Metal Oxide Semiconductor
CMOS	Complementary Metal Oxide Semiconductor
SSN	Simultaneous Switching Noise
SIP	System-In-Package
MCM	Multichip Modules
BGA	Ball Grid Array
EXPO	Expert System for Power Supply

Abbreviation	Description
NEMO	Netlist-based Eission MOdels
PMOS	p-type MOS
NMOS	n-type MOS
DUT	Device Under Test
OATS	Open Area Test Site
TDR	Time-Domain-Reflectrometry
TFF	Toggle Flip-Flop
HDL	Hardware Description Language
TE	Transverse Electric
TM	Transverse Magnetic
EUT	Equipment Under Test
RAM	Radio-frequency Absorbing Material
VNA	Vector Network Analyzer
VSWR	Voltage Standing Wave Ratio
VSWR	Voltage Standing Wave Ratio
CF	Correction Factor
IQR	Interquartile Range

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CHAPTER 1

INTRODUCTION

1.1 General

The electromagnetic compatibility (EMC) of electronic devices is defined as the ability of the device to operate in its own electromagnetic (EM) environment without generating and propagating any excessive EM wave and/or suffering degradation from external electromagnetic interference (EMI) or radio frequency interference (RFI). In general, EMI is an unintentional EM disturbance which may degrade the performance of an electronic device or causes malfunction of the device. Any electronic device must not be susceptible to EMI. This protects correct operation of the devices from spurious emissions such as lightning strikes, electromagnetic pulses (EMP), and the absorption of EMI. The concept is applicable for devices in different levels including system, board, or component levels.

Modern electronic appliances use integrated circuits (ICs) for signal processing due to the benefits of smaller size and lower development cost. An IC, which is also known as a chip or microchip, is a semiconductor device fabricated with thousands or millions of tiny resistors, capacitors and transistors. An IC is considered a miniature set of electronic circuits fabricated on semiconductor materials, such as silicon. In the semiconductor industry, advanced process integration technology and the introduction of new packaging technology at chip scale realized the production of denser ICs with a higher number of I/Os that can operate at a higher frequency. As a result, the IC these days most likely has become a significant noise source that causes EMC problems in electronic devices [1, 2].

A Field Programmable Gate Array (FPGA) chip is a programmable IC that comprises prebuilt programmable logic blocks and reconfigurable interconnects.

Reconfigurable interconnects can be hard-wired to connect different logic blocks together for the execution of any desired digital logic function. The flexibility and rapid prototyping capabilities of the FPGA chip have provided an excellent solution to reach time-to-market constraints in product development, as well as cutting down non-recurring expenses (NREs) cost for the ICs design industry from the beginning. These are the uniqueness of the FPGA chip and why it has been increasingly adopted to replace custom application-specific integrated circuits (ASICs) instead, as processors for signal processing and control applications. Since the invention of programmable technology, its density has grown dramatically from a simple programmable chip into a high density FPGA chip [3]. Therefore, the FPGA chip as well as the modern IC eventually became an ultimate source of EMI that may generate excessive disturbance to interfere with functionality of nearby components or devices [4].

Over the years, EMI concerns at the component level have gained great attention among semiconductor producers [5]. This is due to growing demand by the end user with respect to low emission and high immunity device towards EM disturbance, especially when engaging safety implications in automotive and consumer electronics applications [6]. In particular, the Society of Automotive Engineers has introduced standard SAE J1752/3 [7] for measuring the EM radiation from an IC in 1995. During the following year, the International Electrotechnical Commission (IEC) published standard IEC 61967-2 [8] for the similar purpose. Both standards define evaluation of an IC EM radiation by clamping the IC test printed circuit board (PCB) to a wall port cut in the top or bottom of a TEM or wideband TEM (GTEM) cell. The frequency range of the evaluation is 150 kHz to 1 GHz. Today, both standards are widely accepted by industry and researchers to perform EM radiation from an IC. As ICs require supporting components for operation, it is extremely important to separate the radiation of the IC from its board environment. This is the reason why the standards suggest evaluation by clamping on the cell wall.

The exploration of the IC EM behavior provides vital information for component selection and design concerns in an early product development stage. This can further help to shorten the product development process and avoid additional costs for shielding or filtering prior compliant product EMC requirements.

1.2 Problem Statements

Modern ICs which engage in extraordinary complexity and clock frequency pose vast challenges for product design engineers in developing electronic appliances to comply with product EMC test. Inadequate information on the EM behavior of the ICs is the key factor unworkable of EM simulation involving IC at the early PCB design stage. Therefore, it has become a normal practice for designers to evaluate radiated emission of their design at the end of product development. In this case, the whole design cycle will be repeated if the test is unsuccessful. This happens to require a longer design timeline and the rising of design costs. Evaluation the EM behavior at IC level provides useful information that can be used to facilitate EMI in the design process. With many sophisticated tools available, designers may utilize the information provided to build a model for analyzing product performance at the design level.

The International Standard IEC 61967-2 describes the characterization of ICs radiated emissions using TEM/GTEM cell up to 1GHz. The test setup as described in the standard is clamping the IC test board on a cell wall port so that the IC test board becomes a part of the cell wall. This ensures that the IC is the only radiation source in the measurement and the interference contributed by other noise sources can be avoided. According to the test procedure in the IEC 61967-2, a wall port must be developed at an exact location of a GTEM cell for the IC radiated emission test. Inappropriate wall port integration not only affects the cell characteristics, but it also will upset the accuracy of the measured voltage because it is closely related the spacing between the septum and the test board.

The horizontal positioning of the IC has limited the device rotation in two dimensions across its vertical axis. However, radiated emissions due to the vertical polarization field is also significant [6, 7] and should not be neglected. It is therefore desirable to develop an alternative method to evaluate IC radiated emissions, which account for both horizontal and vertical polarization fields. By performing the emission test inside the GTEM cell, unpredicted fabrication defects can be avoided. In addition, the test device can freely rotate in three orthogonal dimensions for data collection.

Having the IC radiated emission test performed inside the GTEM cell is challenging because the IC requires supporting components for operation. So, the IC under test must firstly be isolated from the disturbance due to the supporting components so that reliability of the measured voltage is attained. The isolation can be done using a metallic enclosure; however, there is a possibility whereby the cavity might be excited as a radiator. Hence, the metallic enclosure must be set up carefully to avoid this situation. The usage of external sources to exercise the IC remains the most crucial matter in the effort to improve repeatability of emission measurement [9]. The unbalanced current on the outer layer of the connection cable causes common-mode radiation and requires further studies for minimizing the cable effects for emission tests in the GTEM cell .

In GTEM cell measurement, the electric field strength cannot be directly measured instead its relative voltage of the field strength is evaluated. Hence, a model must be developed for estimating the actual electric field strength. As the internal structure of the IC is complex, it is difficult to evaluate all the corresponding parameters throughout measurement technique. The dipole moment technique is a unique approach which is suitable for this research. In this technique, an equivalent dipole model is extracted from the GTEM measurement to represent the behavioral aspect of the IC. The advantage is that the model can be constructed without revealing the inner details of the actual circuit. The equivalent model is useful to facilitate EMI of ICs in the design process. Thus, designers may use the model to represent actual activities for analyzing their design alternatively via simulation.

1.3 Objectives of the Research

i. To establish a technique to perform radiated emission measurement of FPGA chip inside a GTEM cell.

ii. To create an equivalent model to represent the radiation sources in the FPGA chip based on dipole moment technique and GTEM cell measurement.

iii. To predict the electric fields of the FPGA using the equivalent model for correlation with semi-anechoic chamber fields.

iv. To validate the predicted electric fields with the measurement in a semi-anechoic chamber.

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