

**ELECTRIC FIELD EMISSIONS OF FPGA CHIP BASED ON
GIGAHERTZ TRANSVERSE ELECTROMAGNETIC CELL
MODELING AND MEASUREMENTS**

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**A thesis submitted in
fulfillment of the requirement for the award of the
Doctoral of Electrical and Electronic Engineering**

**Faculty of Electrical and Electronic Engineering
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JANUARY, 2016

DEDICATION

To my beloved mother and family.



ACKNOWLEDGEMENT

In this thesis, I would like to take this opportunity to express my deepest gratitude to everyone who supported me throughout the journey of PhD study. This thesis would not be completed without the guidance and support from them.

Foremost, I would like to express my sincere gratitude to my supervisor, Professor Dr. Mohammad Zarar bin Mohamed Jenu, who has supported me with his patience, inspiring and invaluable guidances as well as friendly advices during my PhD study. His guidance and encouragement assisted me to overcome many issues and obstacles related to the research activities.

Besides, I would like to thank, Professor Dr. James L. Drewniak for giving an internship opportunity at Missouri University of Science and Technology EMC Laboratory, Rolla, Missouri, United States. The intensive training allowed me to gain experiences and exposure on the latest technology for the integrated circuit field measurement techniques and to learn practical issues which are beyond the scope of the textbooks. Special thanks are addressed to Dr. David Pommerenke, Dr. Jun Fan and Dr. Zhang Yao Jiang, who provided technical advice and insight comments throughout my work to evaluate electromagnetic radiation of integrated circuit and emission modelling along the period of the intensive training at their laboratory.

My sincere thanks also goes to Department of Higher Education, Universiti Tun Hussien Onn Malaysia and Multimedia Development Corporation (MDeC) for providing financial support to undertake my doctorate programme. I also would like to thank Mr Wong Man Onn, Mr Fong Chee Siong and Mr. Ying See Hour from Altera Corporation (M) Sdn. Bhd. for providing FPGA test board, intensive training and technical support on using the Altera Quartus II software and the test board.

Many thanks to my friendly and cheerful group of friends Professor Jing Shen Hui, Professor Gui Liang Qi, Associate Professor Gou Xiang, Ms. Li Jing, Ms. Pan

Jing Nan, Mr. Jackie Ngu and Ms. Ng Ping Ping, whose always willing to help and give their best suggestions in my daily work. I also would like to thank workers in the laboratory, Mr. Sharifunazri bin Johari@Johadi, Mr. Mahmud bin Munajat, and Mr. M. Nazeri bin Sarmijan for assisting me to prepare experimental samples and measurement setup for the investigation.

Last but not the least, I would like to express my greatest appreciation to my mother, madam Ling Kui Ing for her endurance, sacrification and unconditional love for raising me on her own. I also would like to thank my siblings, they always supporting me and encouraging me with their best wishes. Finally, with great sadness and sorrow, I would like to dedicate my greatest blessing to my elder brother, Mr Chua Siew Yiing who has passed away on October 2014. May Almighty God receives his soul with His Love and Mercy.



ABSTRACT

Modern integrated circuits (ICs) are significant sources of undesired electromagnetic wave. Therefore, characterization of chip-level emission is essential to comply with EMC tests at the product level. A Gigahertz Transverse Electromagnetic (GTEM) cell is a common test instrument used to measure IC radiated emission and the test cost is relatively low. Regular IC radiated emission measurements using GTEM tend to neglect some significant emission sources. Thus, this research proposed an alternative methodology to perform field measurement of the IC inside the GTEM cell in order to optimize the field measurements. This research study also attempted analysis of the overall GTEM cell performance using transmission line theory. An FPGA chip was adopted as the IC under test because of its flexibility in configuration to any digital circuit. The investigations discovered that the impact of the FPGA board supporting components and interconnection cables can be significantly reduced with appropriate shielding and grounding. The electric field predict a far distance from the FPGA chip was carried out based on the dipole moment technique. In particular, the dipole moment model emphasizing the tiny horizontal and vertical radiation elements inside the FPGA chip as Hertzian antenna and small current loop. Equations to predict the horizontal and vertical electric field were developed based on Hertzian antenna and small current loop which relate the tiny radiation sources to electric and magnetic dipole moments. The prediction was validated with 3-meter field measurements in a semi-anechoic chamber. On top of that, a spiral-like pattern was developed to obtain a correction factor for further improvement of the correlation between prediction and SAC measurement. The results revealed that the correction factor effectively reduced the gap between the prediction and measurement fields and boosted the correlation coefficient by 44%. The difference of peak values also has limited to less than 10dB after correction. These results suggest a promising finding for a future EMI test of ICs with a cheaper GTEM cell.

ABSTRAK

Litar bersepadu (IC) moden adalah sumber penting menyumbang kepada gelombang electromagnet yang tidak diingini. Oleh sebab ini, penyifatan pengeluaran peringkat cip adalah penting untuk mematuhi ujian EMC di peringkat produk. Sel elektromagnetik melintang gigahertz (GTEM) ialah satu alatan yang biasa digunakan untuk mengukur medan IC yang telah dipancarkan dan kos ujian adalah agak murah. Satu ujian mengukur pancaran medan IC biasa yang dilakukan dengan mengapit papan ujian IC di dinding sel GTEM, yang hamper mengabaikan beberapa sumber pengeluaran penting. Oleh itu, kajian ini telah mencadangkan satu keadah alternatif untuk melaksanakan pengukuran medan IC di dalam sel GTEM untuk mengoptimalkan pengukuran medan. Kajian menganalisa prestasi keseluruhan sel GTEM menggunakan teori talian penghantaran. Cip FPGA telah dipilih sebagai peranti dalam ujian kerana ia fleksible ditatarajah dengan sebarang litar berdigit. Penyiasatan menemui bahawa kesan komponen sokongan papan FPGA dan kabel saling sambung boleh dikurangkan melalui perisaian dan pembumian yang sesuai. Sinaran medan elektrik sepadan pada jarak jauh cip FPGA diramal berasaskan teknik momen dwikutub. Khususnya, model momen dwikutub mewakili sumber pancaran cip yang kecil mendatar dan menegak sebagai antena Hertzian dan gelung arus kecil. Persamaan untuk meramal medan elektrik mendatar dan menegak diterbit daripada antena Hertzian dan gelung arus kecil, dimana sumber pancaran ruas kecil dikaitkan dengan momen dwikutub elektrik dan magnetik. Ramalan ini telah disahkan menggunakan ukuran SAC 3 meter. Untuk penambahbaikan, satu corak pusran dibentuk untuk membangun satu faktor pembetulan bagi tujuan meningkatkan lolerasi antara ramalan dan ukuran SAC. Keputusan mendedahkan bahawa faktor pembetulan adalah berkesan untuk mengurangkan jarak antara medan ramalan dan ukuran dan meningkatkan pekali kolerasi sebanyak 44%. Perbezaan dalam nilai-nilai puncak selepas pembetulan juga telah diambil kira bawah 10dB. Hasil keputusan ini mencadangkan satu pencarian yang menjanjikan satu ujian EMI IC masa hadapan dengan sel GTEM yang lebih murah.

TABLE OF CONTENTS

| | |
|------------------------------------------------------------|------|
| DEDICATION | iii |
| ACKNOWLEDGEMENT | iv |
| ABSTRACT | vi |
| ABSTRAK | vii |
| TABLE OF CONTENTS | viii |
| LIST OF TABLES | xi |
| LIST OF FIGURES | xii |
| LIST OF SYMBOL | xvii |
| LIST OF ABBREVIATION | xix |
| LIST OF APPENDICES | xxi |
| CHAPTER 1 INTRODUCTION | 1 |
| 1.1 General..... | 1 |
| 1.2 Problem Statements | 3 |
| 1.3 Objectives of the Research | 4 |
| 1.4 Scopes of the Research | 5 |
| 1.5 Aim of the Research | 6 |
| 1.6 Significance of the Research..... | 6 |
| 1.7 Outline of the Thesis..... | 7 |
| CHAPTER 2 LITERATURE REVIEW | 9 |
| 2.1 Background..... | 9 |
| 2.2 Development of Digital Logic Technology | 10 |
| 2.2.1 Integrated Circuit Technology | 10 |
| 2.2.2 Field-Programmable Gate Arrays | 12 |
| 2.2.3 FPGA Process Technology | 13 |
| 2.3 A Brief Historical Perspective of IC EMI Research..... | 14 |
| 2.4 Justification of The Research Gap | 16 |
| 2.5 Mechanism of Chip Emission..... | 20 |

| | | |
|--------------------------------------------------------------------------------|------------------------------------------------------------------------------|-----------|
| 2.5.1 | How Integrated Circuit Generates Disturbances..... | 22 |
| 2.6 | GTEM Cell for Emission Measurements..... | 24 |
| 2.6.1 | GTEM Cell Concept | 25 |
| 2.6.2 | IC EMC Testing Standard..... | 26 |
| 2.6.3 | IC Test Board Layout..... | 27 |
| 2.6.4 | Application of GTEM for Emission Measurements | 28 |
| 2.7 | IC Modeling..... | 30 |
| 2.8 | Summary..... | 32 |
| CHAPTER 3 RESEARCH METHODOLOGY AND CALIBRATION..... | | 34 |
| 3.1 | Introduction..... | 34 |
| 3.2 | Development Process..... | 34 |
| 3.3 | The Proposed GTEM Measurement Setup | 39 |
| 3.3.1 | FPGA Test Board..... | 39 |
| 3.3.2 | Logic Circuit Design and Implementation..... | 40 |
| 3.3.3 | Shielding of Test Board | 42 |
| 3.3.4 | Grounding of the Enclosure | 48 |
| 3.3.5 | Radiated Emission Measurement in GTEM Cell..... | 48 |
| 3.4 | Calibration of GTEM Cell Parameters | 50 |
| 3.4.1 | Characteristic Impedance | 50 |
| 3.4.2 | VSWR | 52 |
| 3.4.3 | Return Loss | 53 |
| 3.4.4 | Analyze Impact of Impedance Mismatch Using Transmission Line Theory | 54 |
| 3.5 | Using Comb Generator for GTEM Cell Calibration | 57 |
| 3.5.1 | Conducted Signal Measurement | 58 |
| 3.5.2 | Radiated Signal Measurement..... | 59 |
| 3.6 | Semi Anechoic Chamber Measurement | 62 |
| 3.7 | Summary | 64 |
| CHAPTER 4 MODELING THE FPGA CHIP WITH DIPOLE MOMENT TECHNIQUE | | 65 |
| 4.1 | Introduction..... | 65 |
| 4.2 | Concept of Dipole Moment Technique | 65 |
| 4.3 | Multipole Model of Measured Voltage at GTEM Port..... | 66 |
| 4.4 | Electric Fields Prediction Using Dipole Moments | 73 |

| | |
|---------------------------------------------------------------------|------------|
| 4.5 Summary | 80 |
| CHAPTER 5 ELECTRIC FIELDS MEASUREMENTS AND PREDICTIONS | 81 |
| 5.1 Introduction..... | 81 |
| 5.2 The Relation between Electric Field Intensity and Voltage | 81 |
| 5.2.1 Measurement Approach | 82 |
| 5.2.2 Analytical Formulation | 85 |
| 5.3 GTEM Cell Response with Different Positioning of Test Device.. | |
| | 87 |
| 5.4 Ambient Noise in GTEM Cell | 92 |
| 5.4.1 Grounding of The Enclosure..... | 94 |
| 5.4.2 Suppression with Ferromagnetic Material | 99 |
| 5.4.3 High Quality Interconnection Cable | 102 |
| 5.5 The TFF Pattern for FPGA Configuration..... | 105 |
| 5.6 Orientations of Test Device in Fields Measurements..... | 109 |
| 5.7 Semi Anechoic Chamber Validation | 115 |
| 5.8 Improve Correlation by a Correction Factor..... | 117 |
| 5.8.1 Representation of IC with a Spiral Pattern..... | 118 |
| 5.8.2 Evaluation of Spiral-like Equivalent Circuit..... | 119 |
| 5.8.3 Field Adjustment by Using Correction Factor | 121 |
| 5.9 Summary | 126 |
| CHAPTER 6 CONCLUSIONS AND RECOMMENDATIONS | 127 |
| 6.1 Introduction..... | 127 |
| 6.2 Conclusions..... | 127 |
| 6.3 Contribution of The Research..... | 129 |
| 6.4 Recommendations for Future Works..... | 130 |
| REFERENCES..... | 132 |
| APPENDIX A : Altera EMI Test Board..... | 142 |
| APPENDIX B | 151 |
| APPENDIX C | 153 |
| APPENDIX D | 155 |
| APPENDIX E | 161 |
| APPENDIX F : Comb Generator CGO-520..... | 166 |
| APPENDIX G : Bias Network 11590B | 168 |

LIST OF TABLES

| | |
|------------------------------------------------------------------------------------------------------------------------|-----|
| Table 2.1 : International guidelines for ICs EMC characterization and modelling .. | 16 |
| Table 2.2 : Existing research works that relavent to the scope in the research..... | 17 |
| Table 2.3 : Standards for EMC emission measurement of IC..... | 27 |
| Table 2.4 : Current techniques used to create IC emission model | 30 |
| Table 3.1 : Comparison correlation coefficient before and after considering V_i | 57 |
| Table 4.1 : Coordinate and magnitude for the vector path r_1 and r_2 | 78 |
| Table 5.1 : Specifications of two coaxial cables selected for connecting the cell and spectrum analyzer..... | 104 |
| Table 5.2 : Guidelines to interprete Pearson's correlation coefficient..... | 123 |
| Table 5.3 : Correlation coefficient of predicted and measured fields | 123 |
| Table 5.4 : Variation ranges for the box plot in Figure 5.36..... | 126 |

LIST OF FIGURES

| FIGURE | TITLE | PAGE |
|-------------|----------------------------------------------------------------------------|------|
| Figure 2.1 | Cost and time saving benefits..... | 10 |
| Figure 2.2 | Digital logic technologies [16, 17]..... | 11 |
| Figure 2.3 | Technology trade-off [16]..... | 12 |
| Figure 2.4 | FPGA block structure [16, 17]..... | 13 |
| Figure 2.5 | FPGA process technologies [18]..... | 13 |
| Figure 2.6 | Intentions for the Altera high-end Stratix product [18]..... | 14 |
| Figure 2.7 | Milestone for EMI research focusing on ICs..... | 15 |
| Figure 2.8 | Mechanism of emissions due to current flowing during switching [28]..... | 21 |
| Figure 2.9 | Strong di/dt generation with technology scale down [28]..... | 22 |
| Figure 2.10 | Paths for ICs to generate disturbances [19]..... | 23 |
| Figure 2.11 | Mechanism of direct electric field emission..... | 23 |
| Figure 2.12 | Mechanism for direct magnetic field emission..... | 24 |
| Figure 2.13 | (a) GTEM cell, (b) Cell cross-section [28]..... | 25 |
| Figure 2.14 | (a) TEM wave, (b) GTEM field distribution..... | 26 |
| Figure 2.15 | IC test board; (a) Top view; (b) Side view [8]..... | 28 |
| Figure 2.16 | GTEM cell measurement setup [28]..... | 29 |
| Figure 3.1 | Flow chart for the research methodology..... | 35 |
| Figure 3.2 | FPGA test board (a) top side, (b) bottom side..... | 39 |
| Figure 3.3 | FPGA test board connection..... | 40 |
| Figure 3.4 | Process of TFF circuit..... | 41 |
| Figure 3.5 | Flow chart to develop TFF circuit..... | 41 |
| Figure 3.6 | Testing TFF circuit using built-in in-system sources and probe editor..... | 42 |
| Figure 3.7 | Geometry of an enclosure..... | 43 |
| Figure 3.8 | Cut-off frequencies of metallic enclosure..... | 44 |

| | |
|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----|
| Figure 3.9 : Reflection and attenuation within a shield | 45 |
| Figure 3.10 : Apertures built for interconnection | 46 |
| Figure 3.11 : Shielding the space using gaskets; (a) Structure of gasket; (b) Placement of gasket between metallic enclosure and test board .. | 46 |
| Figure 3.12 : Actual setup of the test device; (a) The FPGA chip is bounded with conductive gasket; (b) Setup of the test board in the enclosure; and (c) Complete setup for emission test | 47 |
| Figure 3.13 : Radiated emission measurement setup in GTEM cell, (a) Illustration of EUT setup in GTEM cell, (b) Actual setup of EUT in GTEM cell ... | 49 |
| Figure 3.14 : Measuring setup of network analyzer | 51 |
| Figure 3.15 : Characteristic impedance versus frequency | 51 |
| Figure 3.16 : VSWR versus frequency | 53 |
| Figure 3.17 : The return loss of GTEM cell | 54 |
| Figure 3.18 : Representation of radiated emissions measurement, (a) GTEM cell setup, (b) Equivalent circuit of the GTEM cell | 55 |
| Figure 3.19 : Comb Generator CGO-520 | 57 |
| Figure 3.20 : Conducted reference signal for CGO-520, (a) Setup for measurement, (b) Corresponding result of the measurement setup..... | 59 |
| Figure 3.21 : Measurement radiated reference signal of Comb Generator; (a) general setup concept; (b) placement of Comb Generator inside the GTEM cell; (c) measurement the radiated reference signal using spectrum analyzer. | 60 |
| Figure 3.22 : Radiated reference signals..... | 61 |
| Figure 3.23 : The radiated emission system of SAC which available at research center for applied electromagnetics; (a) Typical SAC setup for 3m field measurement; (b) Actual setup in SAC for 3m field measurement; (c) The control system for SAC measurement..... | 64 |
| Figure 4.1 : GTEM cell..... | 66 |
| Figure 4.2 : GTEM versus EUT coordinate systems | 69 |
| Figure 4.3 : A Hertzian dipole | 73 |
| Figure 4.4 : A small current loop..... | 74 |
| Figure 4.5 : Real and image sources of image theory | 78 |
| Figure 5.1 : Electric field distribution of two parallel plates | 82 |
| Figure 5.2 : Radiated electric field measurement using E-field probe | 83 |

| | |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|
| Figure 5.3 : HI-6005 isotropic electric field probe | 83 |
| Figure 5.4 : E-field plot against voltage (a) Normal plot, (b) log scale plot..... | 84 |
| Figure 5.5 : Calculate electric field intensity for the incline septum plate | 86 |
| Figure 5.6 : Comparison field strength of measurement and approximation for frequency 200MHz; (a) Normal scale plot; (b) Log scale plot..... | 86 |
| Figure 5.7 : Test circuit..... | 88 |
| Figure 5.8 : Top view for the orientations of test circuit at horizontal position | 88 |
| Figure 5.9 : Actual setup of test circuit in horizontal position, orientation O1 | 89 |
| Figure 5.10 : Side view for the orientations of test circuit at vertical position..... | 89 |
| Figure 5.11 : Actual setup of test circuit in vertical position, orientation O1..... | 89 |
| Figure 5.12 : Radiated emissions of the simple test circuit in various positions and orientations; (a) horizontal position; (b) vertical position..... | 90 |
| Figure 5.13 : Illustration of the fields for two microstrip traces | 91 |
| Figure 5.14 : Noise floor of empty GTEM cell | 93 |
| Figure 5.15 : Comparison of noise level after setup EUT in GTEM cell | 93 |
| Figure 5.16 : Minimizing the enclosure effect by using ground straps; (a) different types of ground straps selected, (b) grounding using copper tape, (c) grounding with wire Setup for analyzing grounding path on emission measurement..... | 95 |
| Figure 5.17 : Comparison noise floor in a GTEM cell by grounding the EUT with different ground straps: (a) before activating the DUT and (b) after activating the DUT | 96 |
| Figure 5.18 : Grounding at P_1 and P_2 using copper tape | 97 |
| Figure 5.19 : Comparison copper tape grounding at different locations; (a) before powering the DUT, (b) after activating the DUT | 98 |
| Figure 5.20 : Equivalent circuit model for a ferrite | 99 |
| Figure 5.21 : Reducing the effect of cables (a) using ferrite beads, (b) bundling all the cables using conductive woven, and (c) wrapping the cable with a flexible ferrite sheet..... | 100 |
| Figure 5.22 : Measurement results corresponding to the cable setup in Figure 5.8, (a) ambient noise level, (b) radiated emissions captured after triggering the DUT with 100 MHz..... | 101 |
| Figure 5.23 : Noise evaluation of empty cell, (a) Cell configuration, (b) Noise level measured..... | 102 |

| | |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|
| Figure 5.24 : Configuration cable RG213 | 103 |
| Figure 5.25 : Sucoflex coaxial cable structure..... | 104 |
| Figure 5.26 : Removing GSM signal using double shielded cable..... | 105 |
| Figure 5.27 : TFF pattern to configure the FPGA chip | 106 |
| Figure 5.28 : Usage of biased RF sinusoidal signal, at 100 MHz frequency to exercise FPGA chip; (a) The setup to create biased RF signal using the bias network; (b) The measurement of the biased RF signal and output of TFF pattern using oscilloscope | 106 |
| Figure 5.29 : TFF pattern after adding tri-state buffer..... | 107 |
| Figure 5.30 : Comparison on the radiated emission measured of enabled and disabled buffer gate; (a) Horizontal position; (b) Vertical position . | 108 |
| Figure 5.31 : IC current loops..... | 109 |
| Figure 5.32 : Actual setup of EUT inside GTEM cell; (a) horizontal position; (b) vertical position | 110 |
| Figure 5.33 : Orientation of FPGA test device in x-axis; (a) 0°; (b) +45°; and (c) -45° | 111 |
| Figure 5.34 : Orientation of FPGA test device in y-axis; (a) 0°, (b) -45°; and (c) +45° | 112 |
| Figure 5.35 : Orientation of FPGA test device in z-axis; (a) 0°; (b) -45°; and (c) +45° | 113 |
| Figure 5.36 : Peak voltages correspond to the FPGA radiation in three orthogonal positions; (a) 0 degree; (b) +45 degree; (c) -45 degree | 114 |
| Figure 5.37 : Radiated emissions measurement setup in SAC | 115 |
| Figure 5.38 : Changing receiving antenna position to account neglected horizontal components; (a) typical antenna setup, <i>H1</i> ; (b) additional antenna setup for SAC measurement, <i>H2</i> | 116 |
| Figure 5.39 : Estimated radiated emission from FPGA chip in GTEM cell as compared to SAC measurement; (a) horizontal electric field component and (b) vertical electric field component..... | 117 |
| Figure 5.40 : Proposed circuitry representative of standard IC for deriving a correction factor. (a) Schematic diagram of test circuitry, (b) Top view, (c) Bottom view..... | 118 |
| Figure 5.41 : Radiated electric field test in SAC, (a) SAC measurement parameters; (b) Actual setup for equivalent SAC measurement..... | 120 |

- Figure 5.42** : Comparison of GTEM estimated fields and SAC measured fields before and after adjustment by using the correction factor. (a) Horizontal component of radiated electric field, (b) Vertical component of radiated electric field..... 122
- Figure 5.43** : The box plot. 124
- Figure 5.44** : The difference between GTEM prediction and SAC measurement before and after taking correction factor into account; (a) horizontal component; (b) vertical component..... 125



LIST OF SYMBOL

| Symbol | Description | Unit |
|------------|--------------------------------------------------------------------|---------------------|
| E | Electric Field Intensity | V/m |
| H | Magnetic Field Intensity | A/m |
| Z | Wave Impedance | Ω |
| Z_0 | Characteristic Impedance | Ω |
| Z_L | Load Impedance | Ω |
| Z_S | Source Impedance | Ω |
| RL | Return Loss | dB |
| P_r | Reflected Power | W |
| P_i | Incident Power | W |
| f_r | Resonant Frequency | Hz |
| δ | Skin Depth | m |
| σ | Conductivity | S/m |
| μ | Relative Permeability | H/m |
| μ_0 | Relative Permeability of Free-Space, $\mu_0 = 4\pi \times 10^{-7}$ | H/m |
| μ_r | Relative Permeability of Material (dimensionless) | |
| Γ | Reflection Coefficient (dimensionless) | |
| θ_r | Phase Angle | degree ($^\circ$) |
| β | Phase Constant | rad/m |
| c | Speed of Light in Vacuum | cm/s |
| V | Voltage | V |
| V_L | Load voltage | V |
| V_i | Input voltage | V |
| F | Electric Force | N |
| q | Electric Charge | C |
| W | Work | J |
| I_D | Differential-mode Current | A |

| Symbol | Description | Unit |
|---------------|------------------------------------------------------|-------------------------------------------------|
| L | Inductance | H |
| C | Capacitance | F |
| E | Electric Field Vector | V/m |
| H | Magnetic Field Vector | A/m |
| a_n | Forward Excitation Coefficient (dimensionless) | |
| b_n | Backward Excitation Coefficient (dimensionless) | |
| k_n | Propagation Constant (dimensionless) | |
| e_n | Normalized Electric Field Component | |
| h_n | Normalized Magnetic Field Component | |
| δ_{mn} | Kronecker Delta Function | |
| J | Current Density | A/cm ² |
| P | Electric Dipole Moment | C.m |
| M | Magnetic Dipole Moment | A.m ² = J/T |
| a | Cell Width | m |
| g | Septum Height | m |
| y | Gap Width | m |
| V_{ij} | GTEM Measured Voltage | dB μ V |
| b_{ij} | GTEM Correspondence Voltage | V ² · m ² /Ω ² |
| e_{0y} | Vertical Electric Field Component at Origin | $\sqrt{\Omega}/m$ |
| η_0 | Intrinsic Impedance of Free Space, $\eta_0 = 120\pi$ | Ω |
| α | Angle Across Vertical Axis Rotation | degree (°) |
| φ | Phase of Moments | rad/m |
| ω | Radian Frequency of Waveform | rad/s |

LIST OF ABBREVIATION

| Abbreviation | Description |
|--------------|-------------------------------------------|
| EMC | Electromagnetic Compatibility |
| EM | Electromagnetic |
| EMI | Electromagnetic Interference |
| RFI | Radio Frequency Interference |
| EMP | Electromagnetic Pulse |
| IC | Integrated Circuit |
| I/O | Input / Output |
| FPGA | Field Programmable Gate Array |
| NREs | Non-Recurring Expenses |
| ASIC | Application-Specific Integrated Circuit |
| SAE | Society of Automotive Engineer |
| IEC | International Electrotechnical Commission |
| PCB | Printed Circuit Board |
| TEM | Transverse Electromagnetic Mode |
| GTEM | Gigahertz Transverse Electromagnetic Mode |
| SAC | Semi-Anechoic Chamber |
| PLD | Programmable Logic Device |
| CPLD | Complex Programmable Logic Device |
| CAD | Computer Aided Design |
| CACA | Computer-Aided Circuit Analysis |
| MOS | Metal Oxide Semiconductor |
| CMOS | Complementary Metal Oxide Semiconductor |
| SSN | Simultaneous Switching Noise |
| SIP | System-In-Package |
| MCM | Multichip Modules |
| BGA | Ball Grid Array |
| EXPO | Expert System for Power Supply |

| Abbreviation | Description |
|--------------|------------------------------------|
| NEMO | Netlist-based Emission MOdels |
| PMOS | p-type MOS |
| NMOS | n-type MOS |
| DUT | Device Under Test |
| OATS | Open Area Test Site |
| TDR | Time-Domain-Reflectometry |
| TFF | Toggle Flip-Flop |
| HDL | Hardware Description Language |
| TE | Transverse Electric |
| TM | Transverse Magnetic |
| EUT | Equipment Under Test |
| RAM | Radio-frequency Absorbing Material |
| VNA | Vector Network Analyzer |
| VSWR | Voltage Standing Wave Ratio |
| VSWR | Voltage Standing Wave Ratio |
| CF | Correction Factor |
| IQR | Interquartile Range |



LIST OF APPENDICES

APPENDIX A : Altera EMI Test Board

APPENDIX B

APPENDIX C

APPENDIX D

APPENDIX E

APPENDIX F : Comb Generator CGO-520

APPENDIX G : Bias Network 11590B



PTTA UTHM
PERPUSTAKAAN TUNKU TUN AMINAH

CHAPTER 1

INTRODUCTION

1.1 General

The electromagnetic compatibility (EMC) of electronic devices is defined as the ability of the device to operate in its own electromagnetic (EM) environment without generating and propagating any excessive EM wave and/or suffering degradation from external electromagnetic interference (EMI) or radio frequency interference (RFI). In general, EMI is an unintentional EM disturbance which may degrade the performance of an electronic device or causes malfunction of the device. Any electronic device must not be susceptible to EMI. This protects correct operation of the devices from spurious emissions such as lightning strikes, electromagnetic pulses (EMP), and the absorption of EMI. The concept is applicable for devices in different levels including system, board, or component levels.

Modern electronic appliances use integrated circuits (ICs) for signal processing due to the benefits of smaller size and lower development cost. An IC, which is also known as a chip or microchip, is a semiconductor device fabricated with thousands or millions of tiny resistors, capacitors and transistors. An IC is considered a miniature set of electronic circuits fabricated on semiconductor materials, such as silicon. In the semiconductor industry, advanced process integration technology and the introduction of new packaging technology at chip scale realized the production of denser ICs with a higher number of I/Os that can operate at a higher frequency. As a result, the IC these days most likely has become a significant noise source that causes EMC problems in electronic devices [1, 2].

A Field Programmable Gate Array (FPGA) chip is a programmable IC that comprises prebuilt programmable logic blocks and reconfigurable interconnects.

Reconfigurable interconnects can be hard-wired to connect different logic blocks together for the execution of any desired digital logic function. The flexibility and rapid prototyping capabilities of the FPGA chip have provided an excellent solution to reach time-to-market constraints in product development, as well as cutting down non-recurring expenses (NREs) cost for the ICs design industry from the beginning. These are the uniqueness of the FPGA chip and why it has been increasingly adopted to replace custom application-specific integrated circuits (ASICs) instead, as processors for signal processing and control applications. Since the invention of programmable technology, its density has grown dramatically from a simple programmable chip into a high density FPGA chip [3]. Therefore, the FPGA chip as well as the modern IC eventually became an ultimate source of EMI that may generate excessive disturbance to interfere with functionality of nearby components or devices [4].

Over the years, EMI concerns at the component level have gained great attention among semiconductor producers [5]. This is due to growing demand by the end user with respect to low emission and high immunity device towards EM disturbance, especially when engaging safety implications in automotive and consumer electronics applications [6]. In particular, the Society of Automotive Engineers has introduced standard SAE J1752/3 [7] for measuring the EM radiation from an IC in 1995. During the following year, the International Electrotechnical Commission (IEC) published standard IEC 61967-2 [8] for the similar purpose. Both standards define evaluation of an IC EM radiation by clamping the IC test printed circuit board (PCB) to a wall port cut in the top or bottom of a TEM or wideband TEM (GTEM) cell. The frequency range of the evaluation is 150 kHz to 1 GHz. Today, both standards are widely accepted by industry and researchers to perform EM radiation from an IC. As ICs require supporting components for operation, it is extremely important to separate the radiation of the IC from its board environment. This is the reason why the standards suggest evaluation by clamping on the cell wall.

The exploration of the IC EM behavior provides vital information for component selection and design concerns in an early product development stage. This can further help to shorten the product development process and avoid additional costs for shielding or filtering prior compliant product EMC requirements.

1.2 Problem Statements

Modern ICs which engage in extraordinary complexity and clock frequency pose vast challenges for product design engineers in developing electronic appliances to comply with product EMC test. Inadequate information on the EM behavior of the ICs is the key factor unworkable of EM simulation involving IC at the early PCB design stage. Therefore, it has become a normal practice for designers to evaluate radiated emission of their design at the end of product development. In this case, the whole design cycle will be repeated if the test is unsuccessful. This happens to require a longer design timeline and the rising of design costs. Evaluation the EM behavior at IC level provides useful information that can be used to facilitate EMI in the design process. With many sophisticated tools available, designers may utilize the information provided to build a model for analyzing product performance at the design level.

The International Standard IEC 61967-2 describes the characterization of ICs radiated emissions using TEM/GTEM cell up to 1GHz. The test setup as described in the standard is clamping the IC test board on a cell wall port so that the IC test board becomes a part of the cell wall. This ensures that the IC is the only radiation source in the measurement and the interference contributed by other noise sources can be avoided. According to the test procedure in the IEC 61967-2, a wall port must be developed at an exact location of a GTEM cell for the IC radiated emission test. Inappropriate wall port integration not only affects the cell characteristics, but it also will upset the accuracy of the measured voltage because it is closely related the spacing between the septum and the test board.

The horizontal positioning of the IC has limited the device rotation in two dimensions across its vertical axis. However, radiated emissions due to the vertical polarization field is also significant [6, 7] and should not be neglected. It is therefore desirable to develop an alternative method to evaluate IC radiated emissions, which account for both horizontal and vertical polarization fields. By performing the emission test inside the GTEM cell, unpredicted fabrication defects can be avoided. In addition, the test device can freely rotate in three orthogonal dimensions for data collection.

Having the IC radiated emission test performed inside the GTEM cell is challenging because the IC requires supporting components for operation. So, the IC

under test must firstly be isolated from the disturbance due to the supporting components so that reliability of the measured voltage is attained. The isolation can be done using a metallic enclosure; however, there is a possibility whereby the cavity might be excited as a radiator. Hence, the metallic enclosure must be set up carefully to avoid this situation. The usage of external sources to exercise the IC remains the most crucial matter in the effort to improve repeatability of emission measurement [9]. The unbalanced current on the outer layer of the connection cable causes common-mode radiation and requires further studies for minimizing the cable effects for emission tests in the GTEM cell .

In GTEM cell measurement, the electric field strength cannot be directly measured instead its relative voltage of the field strength is evaluated. Hence, a model must be developed for estimating the actual electric field strength. As the internal structure of the IC is complex, it is difficult to evaluate all the corresponding parameters throughout measurement technique. The dipole moment technique is a unique approach which is suitable for this research. In this technique, an equivalent dipole model is extracted from the GTEM measurement to represent the behavioral aspect of the IC. The advantage is that the model can be constructed without revealing the inner details of the actual circuit. The equivalent model is useful to facilitate EMI of ICs in the design process. Thus, designers may use the model to represent actual activities for analyzing their design alternatively via simulation.

1.3 Objectives of the Research

- i. To establish a technique to perform radiated emission measurement of FPGA chip inside a GTEM cell.
- ii. To create an equivalent model to represent the radiation sources in the FPGA chip based on dipole moment technique and GTEM cell measurement.
- iii. To predict the electric fields of the FPGA using the equivalent model for correlation with semi-anechoic chamber fields.
- iv. To validate the predicted electric fields with the measurement in a semi-anechoic chamber.

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