14-BIT CMOS HYBRID DIFFERENTIAL DAC FOR HIGH-RESOLUTION SAR ADC USING VLSI IMPLEMENTATION

MATTHEW KHOO KAH WEN

A thesis submitted in
fulfillment of the requirement for the award of the
Degree of Master of Electrical Engineering

Faculty of Electrical and Electronic Engineering
Universiti Tun Hussein Onn Malaysia

NOVEMBER 2022

To my beloved parents, thank you.

ACKNOWLEDGEMENT

The author would like to express his utmost gratitude to his supervisor and co-supervisor, Dr. Nabihah binti Ahmad and Dr. Warsuzarina binti Mat Jubadi, for guiding him continuously throughout his entire project and providing him with professional advice. A strong sentiment of appreciation is also conveyed to all his family members and relatives, who constantly encouraged him and rendered valuable moral support required for him to complete his project successfully. Moreover, the author who like to extend his profound thanks and deep indebtedness to all the professional engineers at MIMOS Berhad, namely Mr. Yuzman bin Yusoff, Mr. Hasmayadi Abdul Majid, Mr. Chia Chieu Yin and Mdm. Noor Shelida binti Salleh, who imparted their knowledge, time and skills to the author, thereby helping him to develop and enhance his project during his six-month attachment at the company.

Furthermore, the author would like to dedicate a strong recognition to university authorities and the Faculty of Electrical and Electronic Engineering (FKEE) for accepting his application to undertake the full-time research course under the Master of Electrical Engineering programme offered by the university. A sincere word of appreciation also goes to the Research Management Centre (RMC) for providing a generous amount of Postgraduate Research Grant (GPPS) during the entire duration of his research programme for him to pay for the services or platforms required for the successful completion of his project. Additionally, the author would like to acknowledge the efforts taken by the panels in assessing his work and providing him with plenty of constructive feedback for him to further improve his project in future ventures.

Last but not least, the author would like to extend his grateful thanks to other significant parties, such as the Cadence and Mentor Graphics vendors for supplying the Virtuoso Cadence software required by the author to design and simulate the circuitry components for his project in order for its objectives to be accomplished successfully.

ABSTRACT

The advent of highly integrated electronic devices with digitalised architectures have paved the way for the innovation of numerous analogue-to-digital converter (ADC) iterations, such as the successive-approximation-register (SAR) analogue-to-digital converters which benefit from the downscaling in complementary metal-oxide-semiconductor (CMOS) technology. In this project, emphasis was placed on the design and optimisation of the digital-to-analogue converter (DAC), as it poses an important block of the SAR ADC circuit. Research on previous DAC architectures have exposed several performance limitations in their designs which include low resolution levels, high power consumptions, as well as large differential non-linearity (DNL) errors that come as a result of poor conversion linearity. Therefore, the 14-bit DAC proposed in this project aims to bridge the research gap through the implementation of a differential hybrid design that has the objectives of achieving high resolution, optimum conversion linearity and low power consumption. The proposed circuit is comprised of two separate single-ended DACs that are designed and simulated in the Cadence Virtuoso software using the Silterra 0.18 μm CMOS process with a 2.1V voltage supply. Each of these single-ended blocks utilised a segmented 10-bit resistor DAC (RDAC) and a 4-bit binary-weighted capacitor DAC (CDAC) to formulate the 14-bit hybrid architecture. Switching procedures were also applied to the sub-DAC circuits to ensure a low-power design was established. Detailed transient simulations implemented at the schematic and post-layout levels indicated that the DAC performed the required conversions at a 14-bit precision and maximum conversion frequency of 2.5 MS/s with peak DNL errors of –0.1612 and –0.8272, respectively. The circuit acquired peak power consumption and Signal-to-Noise Ratio (SNR) of 0.1496 mW and 68.94 dB respectively for the standard voltage supply of 2.1 V. Generally, the optimised circuit is capable of carrying out digital-to-analogue conversions at a 14-bit resolution level with low power consumption and DNL errors, thus verifying the high-performance levels of the proposed DAC.

ABSTRAK

Kemunculan litar elektronik bersepadu dengan seni bina digital telah membuka jalan inovasi untuk pelbagai jenis penukar analog ke digital (ADC), seperti penganggaran penggantian berturut-turut (SAR) penukar analog ke digital terkini yang termanfaat dari pengurangan skala dalam teknologi semikonduktor-logam-oksida pelengkap (CMOS). Dalam projek ini, penekanan diberikan kepada reka bentuk dan pengoptimuman penukar digital ke analog (DAC) disebabkan ia adalah blok penting dalam litar SAR ADC. Penyelidikan mengenai seni bina DAC lama menunjukkan bahawa rekaan itu mempunyai kekurangan dari segi prestasi mereka yang merangkumi tahap resolusi yang rendah, penggunaan kuasa yang tinggi dan ralat pembezaan bukan linear (DNL) yang besar disebabkan oleh kelinearan penukaran yang lemah. Oleh itu, DAC 14-bit yang dicadangkan dalam project ini bertujuan untuk mengatasi jurang penyelidikan melalui pelaksanaan seni bina pembezaan hibrid yang mempunyai objektif untuk mencapai resolusi tinggi, kelinearan penukaran yang optimum dan penggunaan kuasa yang rendah. Litar yang dilaksanakan terdiri daripada dua DAC tunggal yang terpisah yang direka dan disimulasi dalam perisian Cadence Virtuoso menggunakan proses CMOS Silterra 0.18 μm dengan bekalan voltan 2.1 V. Setiap blok tunggal ini menggunakan satu rentetan perintang DAC (RDAC) 10-bit dan satu kapasitor binari berwajaran DAC (CDAC) 4-bit untuk membentuk seni bina hibrid. Prosedur penukaran juga diaplikasikan pada litar-litar sub-DAC untuk memastikan reka bentuk yang berkuasa rendah ditubuhkan. Simulasi sementara terperinci yang dilaksanakan pada tahap skematik dan pasca susun atur telah menunjukkan bahawa DAC melakukan penukaran yang diperlukan pada ketetapan 14-bit dan frekuensi penukaran 2.5 MS/s dengan ralat DNL tertinggi masing-masing sebanyak –0.1612 and –0.8272. Litar ini memperolehi penggunaan kuasa dan nisbah isyarat-ke-bunyi (SNR) bersamaan 0.1496 mW dan 68.94 dB masing-masing untuk bekalan voltan standard sebanyak 2.1 V. Secara amnya, litar yang dioptimumkan mampu melaksanakan penukaran digital ke analog pada tahap resolusi 14-bit dengan penggunaan kuasa dan DNL yang rendah, dengan itu mengesahkan ketinggian prestasi DAC ini.

CONTENTS

LIST OF TABLES

LIST OF FIGURES

LIST OF SYMBOLS AND ABBREVIATIONS

A2	–	2-bit AND Gate
A4	–	4-bit AND Gate
A5	–	5-bit AND Gate
ADC	–	Analogue-to-Digital Converter
ADE L	–	Analogue Design Environment L
c18	–	CMOS 180nm
C_D	–	Dummy Capacitor
CDAC	–	Capacitor Digital-to-Analogue Converter
CMOS	–	Complementary Metal-Oxide-Semiconductor
Cu	–	Unit Capacitance
D	–	Dummy Devices
DAC	–	Digital-to-Analogue Converter
DEM	–	Dynamic Element Matching
DNL	–	Differential Non-Linearity
DRC	–	Design Rule Check
EDA	–	Electronic Design Automation
H	–	High
I	–	Inverter
IC	–	Integrated Circuit
I_R	–	Resistor-String Current
L	–	Low
LSB	–	Least Significant Bit
LVS	–	Layout Versus Schematic
Mbps	–	Megabits per second
MIM	–	Metal-Insulator-Metal
MOM	–	Metal-Oxide-Metal
MOS	–	Metal-Oxide-Semiconductor

MOSFET	–	Metal-Oxide-Semiconductor Field-Effect Transistor
MSB	–	Most Significant Bit
MUX4	–	4-Bit Multiplexer
MUX10	–	10-Bit Multiplexer
NMOS	–	N-Channel Metal-Oxide-Semiconductor
nom	–	Nominal
nto	–	Thick Oxide Nominal Threshold Voltage NMOS
nto_dnw	–	Deep N-well nto
OUT	–	CDAC's Output Port
O2	–	2-bit OR gate
PEX	–	Parasitic Extraction
PHI1	–	Acquire1
PHI1D	–	Acquire1 delay
PHI2	–	Acquire2
PMOS	–	P-Channel Metal-Oxide-Semiconductor
PREAMP	–	Pre-amplifier
pto	–	Thick Oxide Nominal Threshold Voltage PMOS
pto_mf	–	Multi-finger pto
PVS	–	Physical Verification System
PVT	–	Process, Voltage and Temperature
R_B	–	Feedback Resistor
RC	–	Resistance and Capacitance
R-C DAC	–	Hybrid Resistor-Capacitor Digital-to-Analogue Converter
RDAC	–	Resistor Digital-to-Analogue Converter
res	–	Resistor
R_{ON}	–	ON Resistance
RRDAC	–	Resistor-Resistor-String Digital-to-Analogue Converter
SAR	–	Successive-Approximation-Register

SL	–	Sub-String
SM	–	Main String
SNR	–	Signal-to-Noise Ratio
S_r	–	Logic-Controlled Switch
t_c	–	Conversion Period
t_s	–	Settling Time
TG	–	Transmission Gate
to	–	Thick Oxide
V_C	–	Control Voltage
V_{cm}	–	Common-Mode Input Voltage
V_{DAC}	–	DAC's Output Voltage
V_{DD}	–	Input Analogue Voltage
V_{DDA}	–	Higher-Voltage Analogue Supply Rail
V_{DIFF}	–	Output Differential Voltage
V_{GS}	–	Gate-to-Source Voltage
V_{in}	–	Input Voltage
V_{INDAC}	–	Input DAC Voltage
V_{LSB}	–	Smallest Output Analogue Step Size
VLSI	–	Very-Large-Scale Integration
V_{noise}	–	Voltage Level of Background Noise
V_o	–	Output Analogue Voltage
V_{OUTN}	–	Top DAC's Output Voltage
V_{OUTP}	–	Bottom DAC's Output Voltage
V_R	–	Reference Voltage
V_{REF}	–	Voltage Reference Level
V_{REFN}	–	Negative Voltage Reference
V_{REFP}	–	Positive Voltage Reference
V_{signal}	–	Voltage Level of Desired Output Signal
V_{SSA}	–	Lower-Voltage Analogue Supply Rail
W/L		Width and Length

LIST OF APPENDICES

CHAPTER 1

INTRODUCTION

1.1 Background of Study

The continuous advancement in the field of complementary metal-oxide-semiconductor (CMOS) technology has led to the increased demand for low-power and area-efficient analogue-to-digital converters (ADC) for application in various highly integrated instruments as well as other wireless or portable electronic devices [1]. It is also an important feature in modern consumer electronics applications, as its function as a mixed-signal circuit is crucial in converting a continuous analogue input signal into a discrete digital output, which in turn would allow digitally encoded devices to process the analogue signals [2]. With various ADC architectures currently being developed in the modern world, the key area of focus for circuit designers is the implementation of a design that achieves an optimum balance between the trade-offs of speed, power and resolution [3].

In this project, the main research contribution was focused on the design of the digital-to-analogue converter (DAC) component, which posed as an important subset of the full ADC circuit. The overall scheme of the DAC was created with the intention of achieving full compatibility with its corresponding ADC design. With this in mind, the implementation of the DAC was duly carried out in an effective manner, where certain advances in terms of resolution, conversion linearity and power consumption were expected to be made. Once the DAC design was fully completed, which was inclusive of its schematic and layout features, it was then simulated under real conditions in order to test and observe the performance levels of the circuit in regard to other state-of-the-art DAC designs.

The overall function of a DAC is to convert the digital bits of 1's and 0's sent from the ADC into its analogue equivalent value during each conversion cycle, which corresponds to the input voltage level. In other words, the discrete digital values are reformed together by the DAC into a continuous analogue waveform. This makes the DAC an instrumental feature in electronic devices, such as sound systems (explained in a later section), where the digitalised data within the system is required to be converted into an audible analogue output signal. Therefore, the benefits of incorporating high-resolution DACs within these devices provide them with a greater number of convertible digital bits, which leads to a more discrete and precise representation of the analogue waveform.

The implementation of the 14-bit high-resolution DAC in this project was realised via a hybrid architecture that was comprised of a 4-bit binary-weighted capacitor DAC (CDAC) and a 10-bit resistor DAC (RDAC) that was further subdivided into two parallel 5-bit strings. The selection of this 4+10 hybrid design paved the way for a segmented architecture that was capable of extending the DAC resolution by combining different types of sub-DACs (R and C) together. It is also important to note that the number of DAC components tend to increase exponentially with resolution without the presence of segmented circuit arrays [4], which makes the implementation of this feature even more pertinent in high-resolution designs. The work in [5] also supported the fact that a hybrid DAC structure has a proven prowess in its applicability in high-resolution SAR ADCs of 12 bits or greater, thereby making it an attractive feature in the realisation of this project. Moreover, the hybrid architecture has the unique advantage of allowing designers to introduce different types of methods to optimise each sub-DAC based on individual design requirements and other uncorrelated process parameters [4], thereby enabling the overall performance of the full DAC circuit to be adequately enhanced.

1.2 Problem statement

The growing popularity of wireless sensor networks in many modern-day electronic applications has led to the increase in the demand for high-resolution ADCs with superior conversion linearity and accuracy [6]. However, the limitation of low-resolution circuits creates a bottleneck in the advancement of large-scale integrated

circuits and applications requiring high resolutions. Efforts made to enhance DAC resolution often entail a greater number of unity elements to be added to the design, which refers to the specific quantity of components required to achieve the stipulated resolution of the DAC circuitry (e.g., a 10-bit CDAC would require 1024 (2^{10}) capacitive unity elements to attain a resolution of 10 bits) [7]. This increase in unity elements results in stringent matching requirements being imposed on the DAC circuitry [4].

Furthermore, the enforcement of strict matching or linearity requirements on high-resolution DACs often necessitate large devices to be implemented in the circuitry which leads to high power consumption. This is because DACs transistor-based circuitries require larger dimensions (in terms of width and length) to overcome mismatch issues and optimize the circuit to achieve accurate matching and linearity [8]. This performance parameter is crucial in DAC designs to reduce noise levels and glitches in the output voltage, thereby preventing the voltage from distorting too far from its ideal value, which helps maintain it at an accurate level and increasing the signal-to-noise ratio (SNR) of the DAC [2,9]. The work in [10] also supports the concept of the fulfilment of the CDAC linearity requirements at the expense of a larger unit capacitance and higher power consumption. Based on this concept, it can be deduced that linearity performance and power consumption parameters are somewhat opposed to one another, where efforts made to enhance linearity performance comes with the drawback of increased component sizing, which inevitably leads to higher power consumption. Thus, the challenges faced in the design of the said DAC circuits have become relatively apparent, as their implementations require an optimal setting that leverages both linearity performance and power consumption parameters at a balanced point to be established [10].

Upon consideration of the issues stated above, the proposed DAC circuit had the potential of achieving the desired high resolution and strong conversion accuracy criteria with the implementation of the 4+10 segmented hybrid architecture. The separation of the resolution bits across two distinct components via the segmented architecture ensured that fewer components were used in each sub-circuit, which reduced the total number of unity elements across the entire DAC. This feature also helped to relax the matching requirement of each sub-DAC, as the resolution load was not borne by a single component, thereby providing mutual benefits to both these sub-circuits [11]. The improvement in device matching would thus enable the DAC to

acquire a fine balance between the trade-offs of linearity and power consumption, where the required linearity performance can be realistically attained without having to expend a large number of components or significant amounts of power within the design. Moreover, the introduction of a differential architecture that combined two single-ended DACs in a parallel structure had the potential to realize higher conversion linearity and voltage accuracy. This is proven in the works carried out in [1,2,12] where the implementation of a differential circuit enabled the reduction or removal of common mode noise between the two input volage pairs, which in turn increased the SNR and improved the precision of the output voltage. An additional advantage of the differential design is the increased input voltage range available to the circuit which is double than that of the single-ended counterpart [2].

1.3 Objectives

This research embarked on the following objectives that were set prior to the commencement of the project with the intentions of achieving novelty and advancements in key areas of the conducted work:

a) To design a 14-bit differential DAC for a SAR ADC using a hybrid segmented architecture that achieved milestones in several key parameters, which were high resolution, strong conversion linearity and low power consumption.

b) To verify the precise functionality of the designed differential DAC in accordance with the requisite digital-to-analogue conversion operations.

c) To analyse the overall performance of the differential DAC with respect to its achievements in the aforementioned key parameters.

1.4 Scope of Study

The scope of the research is as follows:

a) A Silterra 0.18µm CMOS hybrid differential DAC (without the operational amplifier) was developed to achieve 14-bit resolution and attain power consumption of less than 1.0 mW, with differential non-linearity (DNL) of ±1 LSB across all critical input codes and Process, Voltage and Temperature (PVT) corners. These PVT corners comprised variations in the process speeds of the CMOS transistors and sub-DACs, voltage magnitudes ranging from 1.8–3.3 V, as well as an operating temperature window of –40 ºC to 120 ºC. The PVT scope was determined and implemented as per the specifications set forth via consultation with the design engineers at MIMOS Berhad. The DAC was solely designed without the inclusion of the comparator due to the time constraints posed by the short attachment period at MIMOS Berhad. Furthermore, the efforts to attain a low-power consuming DAC were limited by the voltage as this parameter is directly proportional to the power. Thus, a low-voltage setting would be ideal to keep the power consumption to a minimum but dipping the voltage below 1.8V would lead to the DNL exceeding the stipulated value. Therefore, the optimum range to satisfy both the low-power and low-DNL requirements was between 1.8V and 2.1V.

b) Functional simulations of the differential DAC architecture were conducted using transient simulations, including both schematic-level and post-layout simulations to validate the operability of the DAC circuit in performing the required digital-to-analogue conversions accurately.

c) Detailed evaluations were conducted of all schematic-level and post-layout simulation results to check the fulfilment of the proposed DAC in correlation with key performance parameters.

1.5 Research contribution

The overall DAC circuit proposed in this research work is highlighted with several novelty features which have the contribution potential in the application of contemporary electronic devices that incorporate these superior traits. Firstly, the high-resolution feature of the DAC is realized via the hybrid combination of two segmented

REFERENCES

[1] X. Xin, J. P. Cai, T. T. Chen, and Q. Di Yang, "A 0.4-V 10-bit 10-KS/s SAR ADC in 0.18 μm CMOS for low energy wireless senor network chip," *Microelectronics J.*, vol. 83, no. November 2018, pp. 104–116, 2019, doi: 10.1016/j.mejo.2018.11.017.

[2] M. Y. Ng, "0.18um low voltage 12-bit Successive-Approximation-Register Analog-to-Digital Converter (SAR ADC)," *Proc. 3rd Asia Symp. Qual. Electron. Des. ASQED 2011*, pp. 277–281, 2011, doi: 10.1109/ASQED.2011.6111760.

[3] H. Wei *et al.*, "An 8-b 400-MS/s 2-b-Per-Cycle SAR ADC With Resistive DAC," *IEEE J. Solid-State Circuits*, vol. 47, no. 11, pp. 2763–2772, 2012, doi: 10.1109/JSSC.2012.2214181.

[4] B. Ma, Q. Huang, and F. Yu, "A 12-bit 1.74-mW 20-MS/s DAC with Resistor-String and Current-Steering Hybrid Architecture," pp. 1–6, 2015.

[5] T. Xingyuan, Y. Yintang, Z. Zhangming, and L. Lianxi, "Novel hybrid D/A structures for high-resolution SAR ADCs - Analysis, modeling and realization," *Microelectronics J.*, vol. 42, no. 7, pp. 929–935, 2011, doi: 10.1016/j.mejo.2011.04.016.

[6] M. Savitha and R. V. S. Reddy, "Dual split-three segment capacitor array Design Based Successive approximation ADC for Io-T ecosystem," *Integration*, vol. 69, no. August 2018, pp. 279–288, 2019, doi: 10.1016/j.vlsi.2019.05.004.

[7] Y. Zhang, E. Bonizzoni, and F. Maloberti, "A 10-b 200-kS/s 250-nA Self-Clocked Coarse-Fine SAR ADC," *IEEE Trans. Circuits Syst. II Express Briefs*, vol. 63, no. 10, pp. 924–928, 2016, doi: 10.1109/TCSII.2016.2538139.

[8] D. K. Jung *et al.*, "A 12-bit multi-channel R-R DAC using a shared resistor string scheme for area-efficient display source driver," *IEEE Trans. Circuits Syst. I Regul. Pap.*, vol. 65, no. 11, pp. 3688–3697, 2018, doi: 10.1109/TCSI.2018.2854849.

[9] C. Hui Yi, "A 14-bit Pseudo-Differential Current-Source Resistor-String Hybrif Digital-to-Analog (DAC) Converter with Low Power Consumption," 2017.

[10] M. Saberi, R. Lotfi, K. Mafinezhad, and W. A. Serdijn, "Analysis of power consumption and linearity in capacitive digital-to-analog converters used in successive approximation ADCs," *IEEE Trans. Circuits Syst. I Regul. Pap.*, vol. 58, no. 8, pp. 1736–1748, 2011, doi: 10.1109/TCSI.2011.2107214.

[11] M. R. Kim, Y. O. Kim, Y. S. Kwak, and G. C. Ahn, "A 12-bit 200-kS/s SAR ADC with hybrid RC DAC," *IEEE Asia-Pacific Conf. Circuits Syst. Proceedings, APCCAS*, vol. 2015-Febru, no. February, pp. 185–188, 2015, doi: 10.1109/APCCAS.2014.7032752.

[12] M. Berens, K. Mai, J. Feddeler, and S. Pietri, "A General Purpose 1.8-V 12-b 4-MS/s Fully Differential SAR ADC with 7.2-Vpp Input Range in 28-nm FDSOI," *IEEE Trans. Circuits Syst. II Express Briefs*, vol. 66, no. 11, pp. 1785–1789, 2019, doi: 10.1109/TCSII.2019.2893111.

[13] A. Payra, P. Dutta, A. Sarkar, and S. K. Sen, "Design of a self regulated flash type ADC with high resolution," *IET Conf. Publ.*, vol. 2015, no. CP683, pp. 591–595, 2015, doi: 10.1049/cp.2015.1698.

[14] R. Megha and K. A. Pradeepkumar, "Implementation of low power flash ADC by reducing comparators," *Int. Conf. Commun. Signal Process. ICCSP 2014 - Proc.*, pp. 443–447, 2014, doi: 10.1109/ICCSP.2014.6949880.

[15] A. Sinha, R. Dey, and S. K. Sen, "Design of a novel error detection and correction scheme for pipeline and other multi-stage ADCs with a mono comparator per stage pipeline like architecture," *2016 2nd Int. Conf. Control. Instrumentation, Energy Commun. CIEC 2016*, pp. 93–97, 2016, doi: 10.1109/CIEC.2016.7513742.

[16] F. Rarbi, D. Dzahini, and W. Uhring, "An 8-Bit , 100-MSPS Fully Dynamic SAR ADC for Ultra-High Speed Image Sensor," vol. 12, no. 1, pp. 1–6, 2018.

[17] J. Cai, F. Ran, and M. H. Xu, "IC design of 2Ms/s 10-bit SAR ADC with low power," *Proc. Int. Symp. High Density Packag. Microsyst. Integr. 2007, HDP'07*, pp. 9–11, 2007, doi: 10.1109/HDP.2007.4283644.

[18] W. Guo, S. Liu, and Z. Zhu, "An asynchronous 12-bit 50 MS/s rail-to-rail Pipeline-SAR ADC in 0.18 μm CMOS," *Microelectronics J.*, vol. 52, pp. 23–30, 2016, doi: 10.1016/j.mejo.2016.03.003.

[19] MAXIM, "Understanding SAR ADCs," *MAXIM*, vol. 1080, pp. 1–6, 2001.

[20] A. Agarwal, "Low-Power Current-Mode ADC For CMOS Sensor IC," Texas A&M University, 2005.

[21] A. Xhakoni, H. Le-thai, T. Geurts, G. Chapinal, and G. Gielen, "PTC-Based Sigma-Delta ADCs for High-Speed, Low-Noise Imagers," *IEEE Sens. J.*, vol. 14, no. 9, pp. 2932–2933, 2014.

[22] D. H. Ko, J. H. Jung, Y. G. Pu, S. K. Sung, K. Y. Lee, and C. Nam, "A Design of 14-bits ADC and DAC for CODEC applications in 0.18μm CMOS process," *Proc. - 4th IEEE Int. Symp. Electron. Des. Test Appl. DELTA 2008*, pp. 3–6, 2008, doi: 10.1109/DELTA.2008.124.

[23] K. Chen, M. Nielsen-Lönn, and A. Alvandpour, "Asynchronous clock generator for a 14-bit two-stage pipelined SAR ADC in 0.18 μm CMOS," *NORCAS 2016 - 2nd IEEE NORCAS Conf.*, pp. 3–6, 2016, doi: 10.1109/NORCHIP.2016.7792910.

[24] Maxim Integrated, "Understanding SAR ADCs: Their Architecture and Comparison with Other ADCs," *Maxim*, vol. 1080, pp. 1–7, 2001.

[25] A. Ashraf, S. Ashraf, N. Z. Rizvi, and S. A. Dar, "Low power design of asynchronous SAR ADC," *Int. Conf. Electr. Electron. Optim. Tech. ICEEOT 2016*, pp. 4214–4219, 2016, doi: 10.1109/ICEEOT.2016.7755511.

[26] J. Park, K. Nagaraj, M. Ash, and A. Kumar, "A 12-/14-bit, 4/2MSPS, 0.085mm2 SAR ADC in 65nm Using Novel Residue Boosting," pp. 12–15, 2017.

[27] J. Y. Lin and C. C. Hsieh, "A 0.3 v 10-bit 1.17 f SAR ADC with merge and split switching in 90 nm CMOS," *IEEE Trans. Circuits Syst. I Regul. Pap.*, vol. 62,

no. 1, pp. 70–79, 2015, doi: 10.1109/TCSI.2014.2349571.

[28] P. Harikumar and J. J. Wikner, “Design of a reference voltage buffer for a 10-bit 50 MS/s SAR ADC in 65 nm CMOS,” *Proc. - IEEE Int. Symp. Circuits Syst.*, vol. 2015-July, pp. 249–252, 2015, doi: 10.1109/ISCAS.2015.7168617.

[29] R. S. Gaddam, “A 10-bit Dual Plate Sampling Capacitive DAC With Auto-Zero-On-Chip Reference Voltage Generation,” 2012.

[30] “Digital to Analog Converters (DAC) | Electricalvoice.” [Online]. Available: https://electricalvoice.com/digital-to-analog-converters-dac/. [Accessed: 07-Jan-2022].

[31] Maxim Integrated, “INL/DNL Measurements for High-Speed Analog-to-Digital Converters (ADCs),” *Maxim*, vol. 283, pp. 1–9, 2001.

[32] S. Arar, “What Are the DNL and INL Specifications of a DAC? Non-Linearity in Digital-to-Analog Converters - Technical Articles.” [Online]. Available: https://www.allaboutcircuits.com/technical-articles/understanding-dnl-and-inl-specifications-of-a-digital-to-analog-converter/. [Accessed: 30-Dec-2019].

[33] “Binary Weighted Resistor DAC | Analog-integrated-circuits || Electronics Tutorial.” [Online]. Available: https://www.electronics-tutorial.net/analog-integrated-circuits/data-converters/binary-weighted-resistor-dac/. [Accessed: 28-Jul-2021].

[34] J. Crowe and B. Hayes-Gill, “Choosing a means of implementation,” in *Introduction to Digital Electronics*, 1998, pp. 191–239.

[35] S. Fairooz, P. Thanapal, P. Ganesan, M. S. Prakash Balaji, and V. Elamaran, “Revisiting the utility of transmission gate and passtransistor logic styles in CMOS VLSI design,” *2021 3rd Int. Conf. Signal Process. Commun. ICPSC 2021*, no. May, pp. 276–280, 2021, doi: 10.1109/ICSPC51351.2021.9451645.

[36] P. Vancura, M. Havranek, T. Benka, Z. Janoska, J. Jakovenko, and V. Vrba, “A capacitor DAC for charge redistribution analog to digital converter with successive approximation,” *Proc. Sci.*, vol. 343, no. September, pp. 17–21, 2018, doi: 10.22323/1.343.0094.

[37] J. Liu, Y. Zhu, C. H. Chan, S. W. Sin, U. Seng-Pan, and R. P. Da Silva Martins,

"Uniform Quantization Theory-Based Linearity Calibration for Split Capacitive DAC in an SAR ADC," *IEEE Trans. Very Large Scale Integr. Syst.*, vol. 24, no. 7, pp. 2603–2607, 2016, doi: 10.1109/TVLSI.2015.2509164.

[38] M. Davidovic, A. Nemecek, G. Zach, and H. Zimmermann, "A 20MS/s 11-bit Digital-to-Analog Converter using a combined capacitor and resistor network," *Norchip - 26th Norchip Conf. Form. Proc.*, pp. 85–88, 2008, doi: 10.1109/NORCHP.2008.4738288.

[39] S. H. Yang, K. S. Lee, S. Kim, and Y. M. Lee, "Charge-redistribution DAC with double bit processing in single capacitor," *Electron. Lett.*, vol. 47, no. 5, pp. 312–313, 2011, doi: 10.1049/el.2011.0032.

[40] R. S. Gaddam, K. S. Lee, and C. K. Kwon, "A 10-bit dual-plate sampling DAC with capacitor reuse on-chip reference voltage generator," *Microelectronics J.*, vol. 44, no. 6, pp. 511–518, 2013, doi: 10.1016/j.mejo.2013.03.004.

[41] W. Wang, R. Zhang, and C. Shi, "A 4.7-mW 12-bit 100-MS/s Hybrid DAC," *2018 14th IEEE Int. Conf. Solid-State Integr. Circuit Technol. ICSICT 2018 - Proc.*, no. 1, pp. 18–20, 2018, doi: 10.1109/ICSICT.2018.8565809.

[42] H. Fan, "Effective method to improve linearity of high-resolution SAR ADC," *Microelectronics J.*, vol. 61, no. April 2016, pp. 35–42, 2017, doi: 10.1016/j.mejo.2016.12.010.

[43] P. Vancura, "Design and Classification of IC Layout Mached Structures," Czech Technical University, 2017.

[44] R. L. Geiger, "Oversampled ADCs Layout and Matching Issues," in *EE505: CMOS and BiCMOS Data Conversion Circuits*, 2019, p. 39.

[45] S. V. R. Kaipu, R. K. Srivastava, and M. Goswami, "Design and Layout of a High-Speed High-Resolution Current Steering DAC based on an Optimized Switching Sequence," Indian Institute of Information Technology, Allahabad, 2017.

[46] "The ABCs of ADCs: Understanding How ADC Errors Affect System Performance." [Online]. Available: https://www.maximintegrated.com/en/design/technical-

documents/tutorials/7/748.html. [Accessed: 08-Jan-2020].

[47] T. Dinh, T. Nguyen, H.-P. Phan, V. Dau, D. Dao, and N.-T. Nguyen, "Physical Sensors: Thermal Sensors," in *Reference Module in Biomedical Sciences*, Elsevier, 2021.

[48] "PVT (Process, Voltage, Temperature) - VLSI- Physical Design For Freshers." [Online]. Available: https://www.physicaldesign4u.com/2020/07/pvt-process-voltage-temperature.html. [Accessed: 24-Mar-2021].

[49] S.-I. T. Yadala, "Process-Voltage-Temperature (PVT) Variations And Static Timing Analysis," 2008.

[50] Y. J. Lee, J. Song, and I. C. Park, "Statistical modeling of capacitor mismatch effects for successive approximation register ADCs," *2011 Int. SoC Des. Conf. ISOCC 2011*, vol. 65, no. 11, pp. 3688–3697, 2018, doi: 10.1109/TCSI.2018.2854849.

[51] M. Pelgrom, A. Duinmaijer, and A. Welbers, "Matching properties of MOS transistors," *Nucl. Inst. Methods Phys. Res. A*, vol. 305, no. 3, pp. 624–626, 1991, doi: 10.1016/0168-9002(91)90167-O.

[52] Q. S. I. Lim, A. V. Kordesch, and R. A. Keating, "Performance comparison of MIM capacitors and metal finger capacitors for analog and RF applications," *2004 RF Microw. Conf. RFM 2004 - Proc.*, pp. 85–89, 2004, doi: 10.1109/rfm.2004.1411082.

[53] B. J. Roger Allen and K. Cheng, "Method of making an MIM capacitor and MIM capacitor structure formed thereby," 2012.

[54] S. Mennillo, A. Spessot, L. Vendrame, and L. Bortesi, "An analysis of temperature impact on MOSFET mismatch," *IEEE Int. Conf. Microelectron. Test Struct.*, pp. 56–61, 2009, doi: 10.1109/ICMTS.2009.4814610.

[55] P. Andricciola and H. P. Tuinhout, "The temperature dependence of mismatch in deep-submicrometer bulk MOSFETs," *IEEE Electron Device Lett.*, vol. 30, no. 6, pp. 690–692, 2009, doi: 10.1109/LED.2009.2020524.

[56] Cadence, "Virtuoso Layout Suite XL," in *Cadence Design Systems*, 2016, p. 1.

[57] H. Semat and R. Katz, “Physics, Chapter 25: Capacitance and Dielectrics,” *Robert Katz Publ. Res. Pap. Phys. Astron.*, vol. 1, pp. 267–285, 1958.

[58] M. B. Heaney, “Electrical conductivity and resistivity,” *Electr. Meas. Signal Process. Displays*, no. January 2003, pp. 7-1-7–14, 2003, doi: 10.1201/9780203009406.

[59] A. B. Kahng, J. Lienig, and I. L. Markov, *VLSI Physical Design: From Graph Partitioning to Timing Closure*. Springer Publishing Company, Incorporated, 2011.

[60] A. Arun, “Operational Amplifier Design Layout and Verification,” 2017.

[61] J. Y. Wen, P. H. Chang, J. F. Huang, and W. C. Lai, “Chip design of a 12-bit 5MS/s fully differential SAR ADC with resistor-capacitor array DAC technique for wireless application,” *2015 IEEE Int. Conf. Signal Process. Commun. Comput. ICSPCC 2015*, 2015, doi: 10.1109/ICSPCC.2015.7338762.

[62] “What is the Parasitic Capacitance Effect? | Tempo.” [Online]. Available: https://www.tempoautomation.com/blog/what-is-the-parasitic-capacitance-effect/. [Accessed: 15-Feb-2021].

[63] Saravanan T. K, “Analysis and design of SAR ADC and 3.5 GHz RF Transmitter in 90nm CMOS,” Georgia Institute of Technology, 2010.

[64] B. S. Rikan, D. Y. Choi, R. E. Rad, A. Hejazi, Y. G. Pu, and K. Y. Lee, “12-Bit 5 MS/s SAR ADC with Split Type DAC for BLE Applications,” *Int. Conf. Ubiquitous Futur. Networks, ICUFN*, vol. 2021-Augus, pp. 247–249, 2021, doi: 10.1109/ICUFN49451.2021.9528534.

[65] S. Thirunakkarasu and B. Bakkaloglu, “Built-in self-calibration and digital-trim technique for 14-bit SAR ADCs Achieving ±1 LSB INL,” *IEEE Trans. Very Large Scale Integr. Syst.*, vol. 23, no. 5, pp. 916–925, 2015, doi: 10.1109/TVLSI.2014.2321761.

[66] I. Knausz and R. J. Bowman, “A low power, scalable, DAC architecture for liquid crystal display drivers,” *IEEE J. Solid-State Circuits*, vol. 44, no. 9, pp. 2402–2410, 2009, doi: 10.1109/JSSC.2009.2025341.

[67] S. Naik, B. Patel, C. Poojary, and S. Mande, “Low Power SAR-ADC Using

180nm CMOS Technology," *Int. J. Res. Eng. Sci. Manag.*, vol. 3, no. 9, pp. 150–154, 2020.

[68] Y. Zhu *et al.*, "Split-SAR ADCs: Improved linearity with power and speed optimization," *IEEE Trans. Very Large Scale Integr. Syst.*, vol. 22, no. 2, pp. 372–383, 2014, doi: 10.1109/TVLSI.2013.2242501.

[69] H. Zhu, W. Yang, N. Egan, and Y. Bin Kim, "Calibration technique tracking temperature for current-steering digital-to-analog converters," *Midwest Symp. Circuits Syst.*, no. 2, pp. 1–4, 2014, doi: 10.1109/MWSCAS.2014.6908337.

[70] D. A. Mercer, "Low-Power Approaches to High-Speed Current-Steering Digital-to-Analog Converters in 0.18 µm CMOS," *IEEE J. Solid-State Circuits*, vol. 42, no. 8, pp. 1688–1698, 2007.

APPENDIX E

LIST OF PUBLICATIONS

I. Conference paper titled "Design of a 14-Bit Hybrid DAC for High Resolution Applications in SAR ADCs," 6th IEEE International Conference on Recent Advances and Innovations in Engineering (ICRAIE), 1st–3rd December, 2021, Universiti Teknology MARA Kedah, Malaysia.
Status: Accepted and presented

II. Journal titled "Design of High-Resolution Digital-to-Analogue Converter for 14-Bit Successive Approximation Analogue-to-Digital Converter," Journal of Physics: Conference Series, 2020.
Status: Accepted and published

III. Journal titled "Design Voltage Comparator 14-Bit for Successive Approximation Analogue-to-Digital Converter," Journal of Physics: Conference Series, 2020.
Status: Accepted and published

APPENDIX F

VITA

The author was born on March 18, 1995, in Sitiawan, Perak, Malaysia. He attended secondary school at SMJK Nan Hwa, Sitiawan, and graduated in 2012 before completing his pre-university studies at the same school in 2014. He then enrolled at Universiti Tun Hussein Onn Malaysia (UTHM) in 2015 and graduated with B.Eng. (Hons) in Electronic Engineering in 2019. Within the same year, he undertook the full-time research course under the Master of Electrical Engineering programme offered by the Faculty of Electrical and Electronic Engineering (FKEE) of UTHM. Upon acceptance into this course, he assumed the role of a research assistant in the field of microelectronics, where he received a 23-thousand-ringgit Postgraduate Research Grant (GPPS) sponsored by the Research Management Centre (RMC) of UTHM. His research project pertained to the design and simulation of the schematic components of a 14-bit Digital-to-Analogue Converter (DAC) circuit using the Cadence Virtuoso Analogue Design Environment (ADE) tools, as well as the construction and optimisation of the physical layout of the equivalent DAC circuit. From July to December 2020, he carried out his master's internship at MIMOS Berhad in Kuala Lumpur as a collaboration with this national research institute to further advance his project under the guidance of professional engineers. Furthermore, his research paper was accepted for presentation at the 6th International Conference on Recent Advances and Innovations in Engineering (ICRAIE 2021) organised virtually by the Faculty of Computer and Mathematical Sciences, UiTM Kedah, from 1st to 3rd December 2021. Additionally, he was an active participant of the Virtual International Research and Innovation Symposium and Exposition (RISE) 2021 organised by the Innovation and Commercialization Centre (ICC), UTHM, in September 2021, where the detailed presentation of his project via the requisite competition materials (poster, slides and videos) earned him the gold award for his efforts.