THE EFFECT OF ALLOYING ELEMENT IN LEAD-FREE SOLDERS ON INTERMETALLICS GROWTH WITH ENIMAG SURFACE FINISH

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SPECIAL GRATITUDES TO:

MY BELIEVED PARENT,
Jaidi Bin Ahmad and Robaah Binti Abdul Rafar
For their supports in whole of my life

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ABSTRACT

Surface finish is coated layer plated on a bare copper board of printed circuit board (PCB). Among PCB surface finishes, Electroless Nickel/Immersion Gold (ENIG) finish is a top choice among electronic packaging manufacturer due to its excellent properties for PCB. However, the use of gold element in ENIG is very high cost and the black pad issue has not been resolved. Thus, by introducing an Electroless Nickel/Immersion Silver (ENIMAG) as alternative surface finish hopefully can reduce the cost and offer better properties. The aim of this study is to investigate the effect of alloying element in lead-free solders on interfacial reaction during reflow soldering between Sn-2.5Ag (SA25), Sn-2.5Ag-0.5Cu-1.0Bi (SACB25051), Sn-2.0Ag-0.7Cu-3.0Bi (SACB20073) and Sn-3.4Ag-4.8Bi (SAB3448) with an ENIMAG surface finish. Solder balls with sizes of 500µm diameters were used. All samples were subjected to an isothermal aging process with four different aging times which are 250 hours, 500 hours, 1000 hours and 2000 hours at 150°C. The characteristics of intermetallic compound (IMC) were analyzed by using scanning electron microscopy (SEM), optical microscope (OM) and energy dispersive x-ray (EDX). The results revealed that there is one layer of $(Cu,Ni)_6Sn_5$ IMC was formed at the interface after reflow soldering and a new layer of $(Cu,Ni)_3Sn_4$ IMC has been found after isothermal aging take place. Subsequently, the grain size and thickness of IMC for SACB20073 is smaller and thinner compared to the SACB25051 followed by SAB3448 and SA25. This is due to the existence of Bi element which can reduce the grain size and the growth rate of IMC. The IMC thickness is proportional to the aging duration and IMC morphology for all solders are became thicker, larger and coarser after exposed to isothermal aging. Furthermore, the nanoindentation test had been conducted and ENIMAG was found reliable and suitable as protective layer for PCB. In addition, it is proved that there was electrical connection between solder ball and ENIMAG through conductivity test and the value of conductivity of SA25 is higher than SAB3448, SACB2551 and SACB20073.

ABSTRAK

Kemasan permukaan ialah salutan pada papan litar tembaga untuk papan litar bercetak (PCB). Antara kemasan permukaan PCB, kemasan *Elektroless Nickel / Immersion Gold* (ENIG) merupakan pilihan utama di kalangan pengilang pembungkusan elektronik kerana sifatnya yang sangat baik untuk PCB. Walau bagaimanapun, penggunaan elemen emas dalam ENIG berkos tinggi dan isu pad hitam tidak dapat diselesaikan lagi. Oleh itu, *Electroless Nickel / Silver Immersion* (ENIMAG) diperkenalkan sebagai alternative baru bagi kemasan permukaan untuk mengurangkan kos disamping menawarkan sifat yang lebih baik. Tujuan kajian ini adalah untuk mengkaji kesan elemen aloi dalam pateri bebas plumbum pada pertumbuhan sebatian antara logam semasa proses pengaliran semula antara Sn-2.5Ag (SA25), Sn-2.5Ag-0.5Cu-1.0Bi (SACB25051), Sn-2.0 Ag-0.7Cu-3.0Bi (SACB20073) dan Sn-3.4Ag-4.8Bi (SAB3448) dengan ENIMAG. Bebola pateri berdiameter 500µm digunakan. Semua sampel telah dikaji dengan proses penuaan haba dengan empat masa penuaan yang berbeza iaitu 250 jam, 500 jam, 1000 jam dan 2000 jam pada 150°C. Ciri-ciri sebatian antara logam (IMC) dianalisis dengan menggunakan *scanning electron microscopy* (SEM), *optical microscope* (OM) dan *energy dispersive x-ray* (EDX). Hasil kajian menunjukkan bahawa terdapat satu lapisan $(Cu,Ni)_6Sn_5$ IMC dibentuk semasa proses pengaliran semula dan lapisan baru $(Cu,Ni)_3Sn_4$ IMC telah terbentuk selepas proses penuaan haba. Selain itu, saiz bijian dan ketebalan IMC untuk SACB20073 adalah lebih kecil dan nipis berbanding dengan SACB25051 diikuti oleh SAB3448 dan SA25. Ini adalah kerana kewujudan elemen Bi yang boleh mengurangkan saiz bijian dan kadar pertumbuhan IMC. Ketebalan IMC adalah berkadar terus dengan tempoh penuaan haba dan bentuk IMC untuk semua sampel menjadi lebih tebal, lebih besar dan lebih kasar selepas terdedah kepada penuaan haba. Selain itu, ujian lekukan telah dijalankan dan kebolehpercayaan ENIMAG terbukti dan sesuai sebagai lapisan pelindung untuk PCB. Di samping itu, kewujudan konduktiviti elektrik antara bebola pateri dan ENIMAG terbukti melalui ujian konduktiviti dan nilai konduktiviti SA25 adalah lebih tinggi daripada SAB3448, SACB2551 dan SACB20073.

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CHAPTER 1

INTRODUCTION

1.1 Background of the Study

For many decades, most electrical and electronic components are involved with lead including solder. The common eutectic solder alloy composition using surface mount technology (SMT) solder materials is 63Sn–37Pb. However, it is well-known that lead (Pb) is a neurotoxin and can give bad health effect, such as reproductive problems, digestive problems, muscle and joint pain (G. Chen, Wu, Liu, Silberschmidt, & Chan, 2016). In 2006, after some concerns about the environment and human health, the Restriction of Hazardous Substances Directive (RoHS) and the European Union Waste Electrical and Electronic Equipment Directive (WEEE) has specified a new rule. The rule states that every manufacturer involved with electrical and electronics are prohibited to use lead in electronic products (Ciocci & Pecht, 2006).

The printed circuit board (PCB) surface finish forms a critical interface between the component to be assembled and the bare printed circuit board. Selction of appropriate PCB surface finish plays an important role in developing a reliable packaging technology. It is required to ensure the solderability of metal underplate. The layer of surface finish has to be deposited on copper substrate to act as diffusion barrier and also providing wetting surface. Several alternative surface finishes have been developed over the years and electroless nickel/immersion gold (ENIG) surface finish is the popular choice in electronic packaging. Compared to other finishes, intermetallic compound (IMC) growth between Ni and Sn is slower because of lower dissolution rate of Ni in Sn. ENIG has several advantages as its provides a uniform flat surface finish, an excellent solder attachment process control and high performance (Yoon & Jung, 2008). However, with significant volatility in precious metal pricing and the constant demand for better products at cheaper prices, manufacturer are being driven to search for ways to reduce cost whilst not sacrificing quality.

Other than that, ENIG surface finish has encountered serious reliability problems which are “black pad” issues and *Kirkendall* voids. Black pad is a phenomenon of poor solder joint interfaces and the term black pad arises from the appearance of the affected Ni-P surface when examined under SEM. The black pad appearance is reported to be the result of galvanic attack of electroless Ni during immersion gold plating process. It was reported that this black-pad cause the solder joint failure which is likely caused by the segregation of the phosphorus-rich layer at the interface between Ni and solder. Kirkendall voids are caused by unbalanced inter-diffusion of Cu and Sn at the interface between substrate and solder. Migration of Cu atoms leaves spaces which not filled by Sn atoms due to dissimilar diffusion rates. These spaces then coalesce and form microvoids, which it was revealed, may affect the reliability of solder joints particularly under shock loading condition (Wang, Tsai & Lai, 2012; Long & Toscano, 2013).

Solder joints reliability in electronic devices are one of the key components of the assemblies where reliability concern increases at elevated temperature of operations due to the growth of intermetallic compound (IMC) in the joints, and also the accelerated degradation of the solder alloys (Amalu & Ekere, 2012). Another significant aspect of solder joint processing is a decent understanding of the solder – substrate intermetallic reaction. The intermetallic layer, which is created from this reaction, is essential in order to accomplish good and reliable solder joints. Nevertheless, extreme growth of this intermetallic layer may cause the degradation of solder joint reliability. The formation and growth of intermetallic during solder-board surface finish interaction is influenced by the addition of alloying elements such as bismuth, copper and silver in lead-free solder. It is believed that the addition of the alloying elements results in retardation of IMC growth and subsequently prevents the embrittlement of IMC (Chang, Yang, Tu, & Kao, 2007).

1.2 Problem Statement

The lead-containing solders are widely used in the electronics industry due to their good wettability, low cost, and satisfactory mechanical properties for lifetime performance (Amin *et al.*, 2014). However, legislation prohibiting the use of lead solders has put a tremendous pressure to researchers, as well as electronic manufacturers to find alternative solders. Several lead-free solder alloys appear to have the potential for replacing lead-containing solders including Sn-rich solders, such Sn-Ag or Sn-Ag-Cu for high temperature soldering, and Sn-Ag-Bi or Sn-Ag-Cu-Bi for low temperature soldering (Tulman & Charlotte, 1989; Mahdavifard *et al.*, 2015).

Nowadays, there are many surface finishes applied on printed circuit board (PCB) in the electronics industry. Electroless Nickel/Immersion Gold (ENIG) finish is a surface finish that offers great characteristics for printed circuit board (PCB) and made ENIG to become popular (Yoon & Jung, 2008). Nevertheless, ENIG is a costlier finish because gold is very expensive. Thus, this study tries to propose an alternative surface finish on printed circuit board by using Electroless Nickel/Immersion Silver (ENIMAG), and hopefully it can offer a better property and lower price than ENIG.

Exaggerated growth of IMC in the solders will give long-term effect to the reliability of the solder. Thus, the counteractive action of these phenomena becomes a difficult task and needs to be considered. A few researchers disclosed that a small amount of alloying element such as Bi, In, Sb, and Zn can improve thermal resistance, solder strength or fatigue life because of its solid solution strengthening effect (Kariya & Otsuka, 1998; Wade *et al.*, 2001; Li *et al.*, 2006). Furthermore, since doping element can help to increase the mechanical properties, it is also a probable way to avoid the exaggerated growth of IMC layer (Li *et al.*, 2006; Chang *et al.*, 2007; Siti Rabiatul Aisha *et al.*, 2016).

1.3 Objectives of Study

The objectives of this research are:

a) To assess ENIMAG surface finish via nano-indentation test and examine the effect of alloying elements in lead-free solders on intermetallic compound formed during reflow soldering and isothermal aging on ENIMAG substrate.

b) To measure a material ability in conducting an electric current via an electric conductivity test

1.4 Scope of the Study

This study is conducted by referring to the following scope and limitations:

a) Deposition of ENIMAG surface finish on copper substrates uses an electroless and immersion plating process. ENIMAG surface finish is accessed by indentation test in order to determine the reliability of the coating layer.

b) Formation of solder joints between lead-free solder alloys: Sn-2.5Ag (SA25), Sn-2.5Ag-0.5Cu-1.0Bi (SACB25051), Sn-2.0Ag-0.7Cu-3.0Bi (SACB20073) and Sn-3.4Ag-4.8Bi (SAB3448) with solder ball size of Ø500µm.

c) The conductivity test was conducted in order to ensure a good electric conductivity between ENIMAG surface finish and the solders.

d) Conducting isothermal aging at 150°C for different aging duration (250, 500, 1000 and 2000 hours).

e) Characterization of IMC formed during reflow and isothermal aging using OM, FESEM and EDX.

1.5 Sustainability Element

This study is implemented using lead-free solder rather than leaded solder in order to avoid the toxic production of lead and meet the requirements of environmental and health concerns.

CHAPTER 2

LITERATURE REVIEW

2.1 Electronic Packaging

The protection for electronic equipment from surrounding and the surrounding from electronic equipment is the best description for electronic packaging. Packaging is important on the science of building up interconnections, and a good operating environment for predominantly electrical circuits. It equip the chips with physical support and environmental protection, removes the heat caused by the circuits and supplies the chips with wires to circulate signals and energy (Frear, 2017).

The package has physically experienced numerous changes reacting to the requirements of the integrated circuit (IC), the final product, and surely cost deliberations. In a perfect world, the guidance have consistently been to give a package that completely assist the IC, reacts to mechanical, electrical and heat specification, and then avoids it if viable, and has the package of limit chip performance. The production of packaging is made as little as possible, which is economic and does not serve as a significant percentage of the actual cost (Roberts & Hill, 2007).

Electronics packaging was built with a series of electronic packages. For example, a series of integrated circuits, each in its own electronic package, is soldered onto a circuit board with other devices, such as transistors and capacitors, each of which is also in its own electronic package. Electronic package was also including the circuit board, as it supplies a place and procedure to affix the integrated circuits, transistor and capacitors. Besides, it gives a firm design that will be easily connected to a framework. The framework is another type of electronic package. It supplies the design wanted to bring the circuit boards to a bigger assembly. The bigger assembly is then located into a sheet metal case (Kwak, 2007).

2.1.1 Level of Packaging

Electronic systems are compose of few levels of packaging, with each level having its own devices to interconnect, technologies of interconnection, procedures of heat removal and protection mechanisms. With technologies grows continuously, there is not one special method of classifying the packaging levels. Generally, there are five layers or stages in electronic packaging that join the integrated circuit (IC) and other components (Figure 2.1). The levels are level 0, level 1, level 2, level 3, and level 4 (Lopez-Buedo & J. Boemo, 2002; Jacques, 2017). Detailed descriptions of the levels of interconnection have been summarized in Table 2.1.

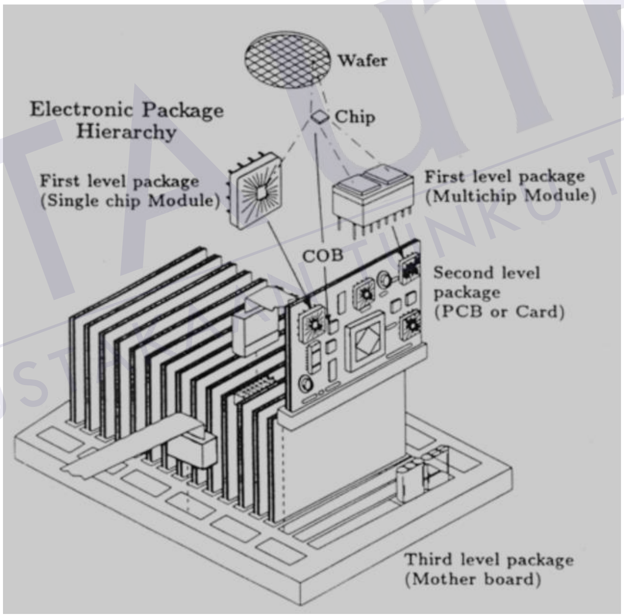

Figure 2.1: Bottom-up packaging and interconnection levels of a generic electronic system (Lopez-Buedo & J. Boemo, 2002)

Table 2.1: Levels of interconnection for general electronic system

LEVEL	DESCRIPTION
Level 0	This level implies interconnecting different electronic component such as diodes, resistors and capacitors on the same chip with no packaging. This microelectronic circuit is called a `bare die' or `bare chip.'
Level 1	Pertains to all processes (mounting, bonding and encapsulating) implied in packaging a bare die to produce an integrated circuit (IC).Wiring the die to a package usually implies one of the interconnection procedure studied in section.
Level 2	Regarding to all the technologies employed in interconnecting a number of such integrated circuits on a printed circuit board (PCB).
Level 3	Regarding to the interconnection of the boards into a cabinet system
Level 4	Regarding to the cabling interconnections and housing of the final system. A typical microelectronic package is designed to provide the following functions: a) Connections for signal lines leading onto and off the silicon chip. b) Connections for power lines that powers the circuits on the chip. c) Connections of signal lines between the system components and interconnections for input/output terminals. d) Removal of the heat generated by the circuits. e) Support and protection of the bare chip.
Level 5	Connections between physically separate systems, using for example an Ethernet LAN

2.2 Surface Finish

A surface finish can be described as a coating, either metallic or organic in nature, which is plated to a printed circuit board (PCB) so as to guarantee solderability of the metal underplate. It is solderability preservative, as the outermost layer mix into the solder paste during soldering process. The surface finish of the PCB, serve as the final step in fabrication before component attachment and the interface between the outer board circuitry and the bonding medium. The use of lead-free solders needs higher soldering temperatures and spots that rise the requirements on the surface finish in order to withstand multiple reflow cycles (Vianco, 1999).

The surface finishes of printed circuit board (PCB) produce a critical interface between the bare copper and electronic component. Figure 2.2 shows the cross-sectional view of surface finish and bare copper. This surface finish has three primary functions. First, it acts as a protection for underlying copper from oxidation. Secondly, it functions as a diffusion barrier to avoid exaggerates IMC formation between the solder and the substrates. Lastly, surface finish is used to provide and improve solderability and wettability of the surface (Amagai, 2002).

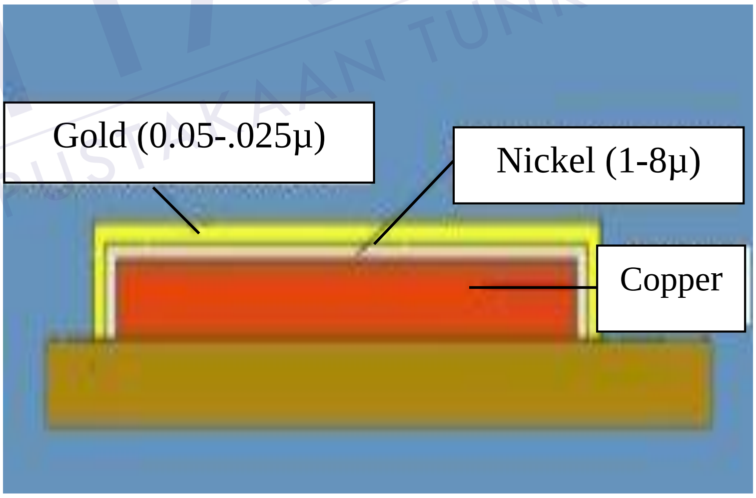

Figure 2.2: Surface finish deposition (Amagai, 2002)

2.2.1 Coating Thickness

The thickness of the surface finish and coating layers must be firmly controlled. The most decisive thing to be controlled for the solderable layer is managing the definite minimum layer thickness. Generally, the molten solder begins to dissolve the solderable finish on substrate. Thin layer is preferable for the recommended time interval of the molten solder contacts, and it will be fully dissolved during the soldering process, accordingly uncovering the molten solder to the fundamental base material surface. Due to the reason of the solderable layer to accommodate an unsolderable base material surface, there is no reason to accept that the base material surface has been made solderable, either intentionally or by means of the plating process. In fact, it should always be assumed that the fundamental base material surface is not solderable. When the molten solder meets the unsolderable base material surface, the molten solder de-wets from the surfaces (Nable, 2015; Vianco, 1999).

When specifying the thickness of the solderable layer, it is important to also consider subsequent soldering steps (repair and rework tasks) that will cause additional solderable layer dissolution. Finally, a limited amount of consumption of the solderable layer also occurs by solid-state intermetallic compound layer growth between the layer and the solder. Full transformation of the solderable finish into an intermetallic compound jeopardizes the integrity of the joint, as there is no assurance that the intermetallic compound layer adheres to the base metal surface. Surface finishes generally have their own common thickness. It is important to ensure the surface finishes provide enough solderability of the surface (Lamprecht, 2005; Nable, 2015; Vianco, 1999). The common thicknesses of surface finishes are shown in Table 2.2.

Table 2.2: Common thickness of surface finishes (Nable, 2015)

Surface finish	Thickness, µm
HASL	0.65-60/(25-2000)
ENIg	2.5-5/(100-200)Ni and 0.05-0.23/(2-9)Au
ImAg	0.15-0.45/(6-8)Ag
ImSn	0.6-1.6/(25-60)Sn
OSP	0.2-0./6(8-24)
ENEPIG	25/100-200)Ni, 0.2-0.6/(8-24)Pd and 0.2-0.05(1-2)Au

It is important to ensure that dissolution of solderable finish could weaken the properties of the molten and solidified solder. Nonetheless, such situations are hardly found, this is due to the purpose that traditional solderable finishes (e.g. Ni, Pd, and Fe) have approximately low dissolution rates in molten solder (Bewlay & Gigliotti, 1997; Zhu, 2014; Adawiyah *et al.*, 2016). Figure 2.3 shows the dissolution rates of several metals in tin.

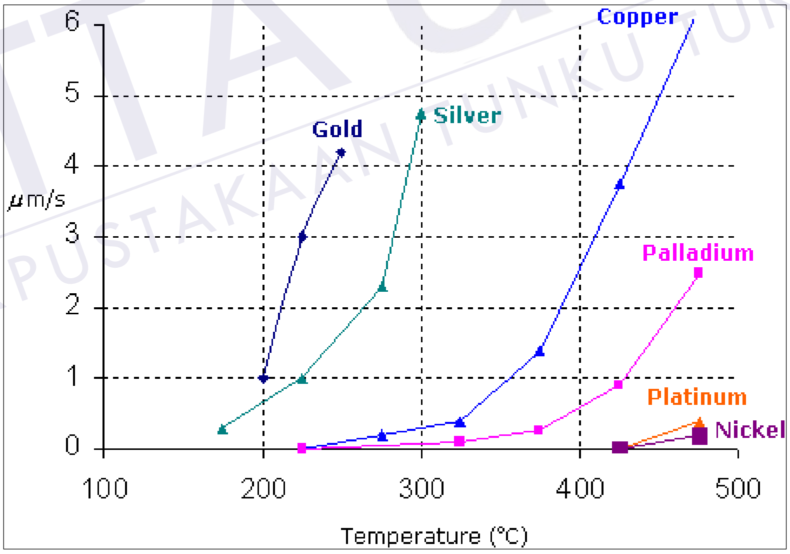

Figure 2.3: Dissolution rates of a few typical base metals in tin (Zhu, 2014)

Exaggerate thick solderable layer have two major defects. Firstly, defect on the technically based. All coating layer are plated with certain levels of residual stress and contamination, the latter increasing from bath components. The extent of every one of these variables increments as the layer thickens. Excessively thick layers have higher residual stresses that can be a cause of delamination by the layer

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