MODELLING OF ADVANCED SUBMICRON GATE InGaAs/InAlAs pHEMTS AND RTD DEVICES FOR VERY HIGH FREQUENCY APPLICATIONS

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LIST OF ABBREVIATIONS

2DEG	Two-Dimensional Electron Gas
ADS	Advanced Design System
ASKAP	Australian SKA Pathfinder
ATA	Allen Telescope Array
CAD	Computer Aided Design
CMOS	Complementary Metal Oxide Semiconductor
CPW	Coplanar Waveguide
DC	Direct Current
HBT	Heterojunction Bipolar Transistor
HEMT	High Electron Mobility
ICCAP	Integrated Circuit Characterization and Analysis Program
IF	Intermediate Frequency
LNA	Low Noise Amplifier
MBE	Molecular Beam Epitaxy
MESFET	Metal Semiconductor Field Effect Transistor
MMIC	Monolithic Microwave Integrated Circuit
MOCVD	Metal-oxide Chemical Vapour Deposition
MODFET	Modulation Doped FET
M&N	Microelectronic and Nanostuctures
NF	Noise Figure
NF_{min}	Minimum Noise Figure
pHEMT	Pseudomorphic High Electron Mobility Transistor
PNA	General-purpose Network Analyser
QW	Quantum Well
RF	Radio Frequency
RTD	Resonant Tunnelling Diode

SDHT	Selectively Doped Heterostructure Transistors
SKA	Square Kilometre Array
TEGFET	Two Dimensional Electron Gas Field Effect Transistors

Notations

$C_{ds,gs}$	Drain/gate to source capacitance
C_{gd}	Drain to gate capacitance
$C_{pg,pd,ps}$	Pad capacitances to electrodes
ΔE_c	Conduction band discontinuity
ΔE_g	Band gap difference of heterojunction materials
ΔE_c	Valence band discontinuity
E_g	Band gap energy
E_{br}	Breakdown voltage
E_{fn}	Electron Quasi fermi level
E_F	Fermi Level
$L_{g,s,d}$	Gate/Source/Drain contact inductance
N_C	Effective density of states
P	Polarization
P_{sp}	Spontaneous polarization
P_{pz}	Piezo-electric polarization
q	Electron charge
$R_{g,s,d}$	Gate/Source/Drain contact resistance
Rds,gs	Drain/gate to source resistance
v_{sat}	Saturation velocity
V_T	Threshold voltage of HEMT
$xAlGaN$	Aluminium molefraction in GaN
μ	Carrier Mobility

ABSTRACT

The University of Manchester
Candidate: Warsuzarina binti Mat Jubadi
Degree: Doctor of Philosophy (PhD)
Thesis Title: Modelling of Advanced Submicron Gate InGaAs/InAlAs pHEMTs and RTD Devices for Very High Frequency Circuits
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InP based InAlAs/InGaAs pseudomorphic High Electron Mobility Transistors (pHEMTs) have shown outstanding performances, which makes them prominent in high frequency mm-wave and submillimeter-wave applications. However, conventional InGaAs/InAlAs pHEMTs have major drawbacks, i.e., very low breakdown voltage and high gate leakage current. These disadvantages degrade device performance, especially in Monolithic Microwave Integrated Circuit (MMIC) low noise amplifiers (LNAs). The optimisation of InAlAs/InGaAs epilayer structures through advanced bandgap engineering together with gate length reduction from 1 μm into deep sub-μm regime is the key solution to enabled high breakdown and ultra-high speed, low noise pHEMT devices to be fabricated. Concurrently, device modelling plays a vital role in the design and analysis of pHEMT device and circuit performance. Physical modeling becomes essential to fully characterise and understand the underlying physical phenomenon of the device, while empirical modelling is significant in circuit design and predicts device's characteristic performance.

In this research, the main objectives to accurately model the DC and RF characteristics of the two-dimensional (2D) physical modelling for sub-μm gate length for strained channel InAlAs/InGaAs/InP pHEMT has been accomplished and developed in ATLAS Silvaco. All modelled devices were optimised and validated by experimental devices which were fabricated at the University of Manchester; the sub-micrometer devices were developed with T-gate using I-line optical lithography. The underlying device physics insight are gained, i.e, the effects of changes to the device's physical structure, theoretical concepts and its general operation, hence a reliable pHEMT model is obtained. The kink anomalies in I-V characteristics was reproduced and the 2D simulation results demonstrate an outstanding agreement with measured DC and RF characteristics.

The aims to develop linear and nonlinear models for sub-μm transistors and their implementation in MMIC LNA design is achieved with the 0.25 μm $In_{0.7}Ga_{0.3}As/In_{0.52}Al_{0.48}As/InP$ pHEMT. An accurate technique for the extraction of empirical models for the fabricated active devices has been developed and optimised using Advance Design System (ADS) software which demonstrate excellent agreement between experimental and modelled DC and RF data. A precise models for MMIC passive devices have also been obtained and incorporated in the proposed design for a single and double stage MMIC LNAs in C- and X-band frequency. The single stage LNA is designed to achieve maximum gain ranging from 9 to 13 dB over the band of operation while the gain is increased between 20 dB and 26 dB for the double stage LNA designs. A noise figure of less than 1.2 dB and 2 dB is expected respectively, for the C- and X-band LNA designed while retaining stability across the entire frequency bands.

Although the RF performance of pHEMT is being vigorously pushed towards terahertz region, novel devices such as Resonant Tunnelling Diode (RTD) are needed to support future ultra-high speed, high frequency applications especially when it comes to THz frequencies. Hence, the study of physical modelling is extended to quantum modelling of an advanced $In_{0.8}Ga_{0.2}As/AlAs$ RTD device to effectively model both large size and submicron RTD using Silvaco's ATLAS software to reproduce the peak current density, peak-to-valley-current ratio (PVCR), and negative differential resistance (NDR) voltage range. The simple one-dimensional physical modelling for the RTD devices is optimised to achieve an excellent match with the fabricated RTD devices with variations in the spacer thickness, barrier thickness, quantum well thickness and doping concentration.

1 CHAPTER 1

INTRODUCTION

1.1 Overview

The High Electron Mobility Transistor (HEMT) and Pseudomorphic High Electron Mobility Transistor (pHEMT) are Field Effect Transistors (FET). HEMTs operate in a similar manner to MESFET but extend the performance of FET by taking advantage of the large band discontinuities in the band structures of the constituent semiconductor materials. Basically, HEMTs structure consists of compositional compound materials that are lattice-matched to the substrate. However in the pHEMT structure, the channel material is so thin that the crystal lattice stretches "pseudomorphically" to occupy the spacing of the nearby material. Consequently, it allows better performance due to the larger bandgap difference compared to the lattice-matched structure. The formation of quantum well and the two dimensional electron Gas (2DEG) in the channel provides HEMT with a high electron mobility and high carrier density, leading to low noise figures and higher cut-off frequency [1].

Amongst all material systems in the III-V compound semiconductors, the InGaAs/InAlAs material system has the most desirable band structure and transport properties (carrier mobility, saturation velocity, etc). This material system offers pHEMT devices with high electron sheet charge density and excellent carrier confinement in the channel, resulting in superior electron transport translating into higher transconductance (g_m), current gain cutoff frequency (f_T) and lower noise figure (NF). Hence, the InGaAs/InAlAs has become an advanced material system for high-speed, high-frequency and even in the lower frequency range of 0.9 GHz and 1.9 GHz that are used for mobile communication [2]. Current development of InP based InAlAs/InGaAs HEMTs have demonstrated excellent high frequency and high-gain performance [3, 4], i.e. a cut-off frequency above 625 GHz [5], and they dominate the microwave and millimetre wave applications and low noise amplifiers (LNAs) fields [6, 7, 8].

The superior performance of InP based InAlAs/InGaAs pHEMTs as compared to the GaAs-based HEMT [9] makes them the most preferred candidates for the active devices selection and also an important aspects in the fabrication of Monolithic Millimeter Wave Integrated Circuit (MMIC) LNAs. The design of MMIC LNAs itself has emerged from the design for very low frequency, low noise figure, very high power, etc. For over a decade, the advancement in millimeter wave semiconductor technologies has been strongly driven by military requests such as sensor/radar application [10]. There are also an increasing number of wireless civil applications, i.e telecommunication-, sensors- and navigation-systems that are ever demanding for more and more low-noise and power devices at high frequencies. Undoubtedly, these systems could be realised with the outstanding combination of high frequency operation and low noise performance of the InGaAs/InAlAs/InP pHEMT devices.

1.2 Project Motivation and Objective

Recent advances in Metal Organic Chemical Vapour Deposition (MOCVD) and Molecular Beam Epitaxy (MBE) epitaxial growth techniques for III-V compound semiconductor systems have made it possible to grow extremely high-quality III-V heterojunction structures. Current development of InAlAs/InGaAs HEMTs have demonstrated excellent high cutoff frequency of 625 GHz up to 1 THz and high-gain performance [3, 4] and dominate the millimeter wave applications, i.e., low cost LNA [3] and Ka-band MMIC LNAs [6]. The previous work conducted by the Manchester group on novel pHEMT devices [11,12] and hence the MMIC LNA development for the SKA was initiated at the SKA-low frequency (L-band) [13, 14] using a one micron gate length device.

With the device size scaled down to the nanometer regime and various epitaxial layer structures being designed and optimized, physical modeling becomes essential to fully characterize and identify the underlying physical phenomenon of these devices. Semiconductor modelling based on physical models [15, 16] can prove to be very helpful in the development of such transistors. The empirical modelling [17,18] is also required to accurately model and estimate the performance analysis the linear and nonlinear behaviour of the designed circuits , i.e. LNA over a range of frequency and characterize the device technological process. The development and verification of device simulation tools have become desirable as to compare statistically analysed measured data. With the aid of modelling, the time and cost of device fabrication and characterization undoubtedly can be considerably reduced [19]. This research aims to employ the advances of modelling tools, SILVACO simulation package and Advanced Design System (ADS) to appreciate the underlying device physics of the device towards the device output characteristics, to reproduce both the DC and RF device characteristic, and investigate the correlation of the device physics to the output characteristics. The initial work of the device modelling of 1 μm gate device will be extended to the deep submicrometer gate regime and aim to develop models for new transistors and their implementation in the design and fabrication of advanced integrated circuits using the extensive facilities available at the University of Manchester.

Despite of the high cut-off frequency achievements reported for InP pHEMT in the terahertz region, i.e. [20] and [21], novel devices are needed which are able to support future ultra-high speed, high frequency applications; especially when it comes to sub-THz or THz frequencies (operating at room temperature). The Resonant Tunnelling Diode (RTD) might well be the solution to this problem with its ability to provide a very high fundamental frequency well into the THz region. Therefore, the study of physical modelling is extended to quantum modelling for an advanced InGaAs/AlAs RTD device. The purpose of this extended work is to effectively model the RTD using Silvaco's ATLAS software; particularly with respect to the peak current density, peak-to-valley-current ratio (PVCR), and negative differential resistance (NDR) voltage range.

1.3 Scope of thesis

This thesis presents the physical and empirical modelling of advanced InGaAs/InAlAs pHEMT for the development of low noise amplifier (LNA) designs to fulfil the requirements of the (8.0 to 12 GHz) band of the Square Kilometre Array (SKA) [22]. During the preliminary work, the transistor used in this project employed a 1µm gate length with multiple sized gate widths. The modelling and circuit designs are then progressed with the submicrometer gate InGaAs/InAlAs pHEMT to facilitate higher frequency applications. The transistors were in-house fabricated at the University of Manchester and the measurement of the transistors is carried out at room temperature. The proposed design is a Monolithic Microwave Integrated Circuit (MMIC) that combine high performance with low cost and avoids expensive and labor intensive external components (especially discrete inductors used for the input of the LNA). In this work, the advances in the InGaAs/InAlAs material system is fully utilised in the submicron gate length pHEMT and the study is extended into a simpler one dimensional structure of a two terminal device, the InGaAs/AlAs resonant tunnelling diode (RTD).

1.4 Thesis Outline

The organization of the remainder of this thesis is as follows:

Chapter 2 provides insights into the fundamental theory of semiconductor device physics for heterojunctions and HEMTs structure background. This chapter deals with the literature review of the basic concepts of III-V compound semiconductors. The development of different III-V FET devices in relation to the advancement of material engineering and their contribution to RF applications are presented. A comparison between the different FET structures (MESFET, HEMT and pHEMT) and material systems (InGaAs-AlGaAs, InGaAs-InAlAs) and the advantage of InP-based pHEMT for low noise and high speed applications is outlined. The discussion continues with an extensive study of the physics and operation of the devices. At the end of the chapter, some important physical parameter extraction methods are highlighted, as these methods are used throughout this work.

Chapter 3 highlights the significance of device simulations, introduces the simulation tools used in the development of the physical modelling performed in this work. Detail procedures of the device modelling of pHEMTs structure are presented, i.e. meshing, structure and parameter definitions, and physical models, and numerical methods. A detail explanation of the concepts of device modelling and current-transport equations used in this project is presented.

Chapter 4 briefly explains the fundamental models that are used in the simulation work for the small signal model. In this chapter a physically based model for various samples of the in-house fabricated pHEMTs has been developed, providing an insight to the internal device behaviour. The DC and RF characteristics of the two dimensional physical device simulations are compared with the experimental results which were fitted and analysed. The modelled device simulation shows excellent agreement with the experimental results.

Chapter 5 explains the empirical model parameters and device modelling steps for the pHEMT device. The empirical models for three different epitaxial layers with various device sizes and gate length are presented. The agreements between the modelled and measured parameter are discussed and analysed. An optimized pHEMT model which is used in the LNA design and a brief study on the device's noise characteristics are presented at the end of this chapter. The results from device empirical modelling provides a guide for active device selection for LNA circuit designs.

Chapter 6 begins with the background of Monolithic Microwave Integrated Circuit (MMIC) and its advantages in the integrated circuit roadmap. This is followed by an outline of the LNA theoretical concept which is used to examine the requirements of a complete system design. The target specifications of the MMIC LNA design are then addressed; the performance constraints and compromises that arise in the design of circuit topologies, biasing networks and matching configurations are also discussed. The design and analysis of the single input single-ended output, single and double stage LNAs are presented using all of the criteria discussed in Chapters 6. The LNAs are designed to match a 50 Ω input and output impedance. At the end of this chapter, the target specifications attained from the simulation of the single- and double-stage MMIC LNA for C-band and X-band frequency range are presented and discussed. The layout designs of these LNA circuits are also developed and presented.

Chapter 7 demonstrates a one-dimensional physical modelling for various sample of large-siz and submicrometer $In_{0.8}Ga_{0.2}As/GaAs$ Resonant Tunneling Diode (RTD) device. The concept, operation principle and the applications of RTD in Terahertz (THz) region are explained at the beginning of the chapter. The modelling of the two terminal RTD device focuses on the DC analysis, which is mainly to reproduce the I-V characteristics of experimental devices, namely the negative differential resistance (NDR), NDR peak voltage, V_P (voltage at peak current) and the peak current density(I_P). The model optimisation based of the device structure, i.e. spacer layer, barrier layer and quantum well layer thicknesses are also studied. The modelled device simulation for DC analysis shows excellent agreement with the experimental results.

Finally, **Chapter 8** summarises the work that has been discussed in the earlier chapters and suggests some potential future research to further extend the work described in this thesis.

2 CHAPTER 2

THEORY AND BACKGROUND OF PSEUDOMORPHIC HIGH ELECTRON MOBILITY TRANSISTOR

2.1 Introduction

For the past decades, the power of electronics has been driven by an increase in the density of silicon complementary metal–oxide–semiconductor (CMOS) transistors and the progression to their logic performance. The semiconductor chips are becoming more powerful, smaller and more economical and energy efficient. However, as the scaling of silicon transistor is now reaching its limits, the III-V compound semiconductors are now becoming the key choice to continue the microelectronic revolution for high speed and high frequency devices. The outstanding electron transport properties and frequency response of these materials might be central to the development of nanometre-scale logic transistors [23]. For example, the electron mobility in InGaAs and InAs HEMT is more than 10 times higher than in silicon at a comparable sheet density. In the early development, HEMTs, also known as Modulation Doped Field Effect Transistors (MODFETs), Two-dimensional Electron Gas Field Effect Transistors (TEGFETs), Heterojunction Field Effect Transistors (HFETs) or Selectively Doped Heterostructure Transistors (SDHTs) was originally developed for high speed applications and these devices were discovered to exhibit a very low noise figure. This is related to the nature of the two-dimensional electron gas (2DEG) and the fact that there are less electron collisions in the channel [6].

The basic fundamental which govern the development of HEMTs are explained in this chapter. An introduction to heterojunction, their band structures, formation of quantum wells, carrier confinement and 2DEG will be discussed. The HEMT and pHEMT structures and their operational principles are summarized. Some of the applications of pHEMTs and works concentrating in the pHEMTs design in the literature are also highlighted in later sections.

2.2 Hetero Junction Structure

Generally, HEMT structures are based on epitaxially grown layers with different compositions and energy band gaps. When these different semiconductor layers are brought together, they form heterojunctions. The principle parameters for heterostructures are the difference of energy bandgaps (*Eg)* and the lattice constant (*a)* for the two semiconductor materials. Figure 2.1illustrates the lattice constant and energy gap parameters for various III-V material system that are of interest to the work presented here. These parameters play a very important role in the advanced bandgap engineering to optimize device characteristics.

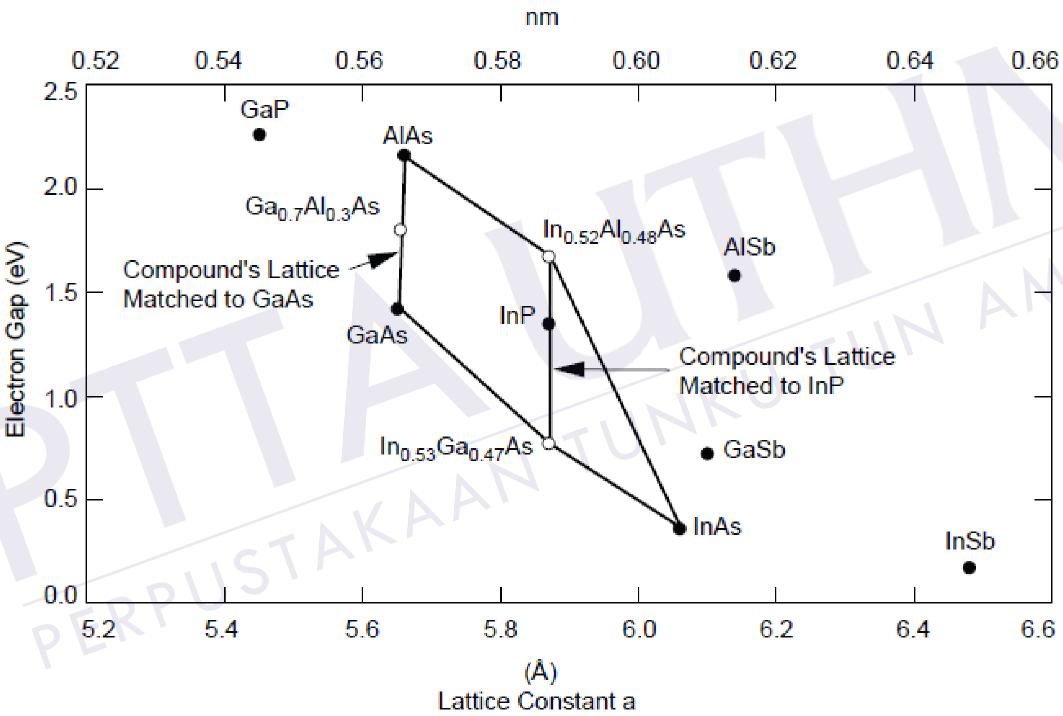


Figure 2.1 The energy gap of III–V compounds and ternary derivatives as a function of lattice constant [24]

The ternary compound semiconductor materials that are lattice matched to GaAs and InP substrates are shown. For example, the AlAs, $Al_xGa_{(1-x)}As$, (for all values of x) and $In_{0.48}Ga_{0.52}P$ is lattice match with GaAs. Consequently, the $In_xGa_{(1-x)}As$ and $In_xAl_{(1-x)}As$ are lattice matched to InP only at a single fixed mole fraction (x ~0.52). Practically, the materials chosen must have a very close lattice constant to minimise the disturbance at the heterointerface. However, for various materials that have slightly different lattice constant, Vegard's law is used to synthesize new semiconductor materials to match the size of the crystal lattices. Therefore, the resulting lattice constant and the energy band gap can be approximated using Vegard's law [21, 22] as in Equation 2.1, where *x* is the mole fraction and *AZ* and *BZ* are the binary compound lattice constant and band gap values,

$$a_{alloy} = x\mathrm{AZ} + (1-x)\mathrm{BZ} \qquad \text{Equation 2.1}$$

The lattice constant and band-gap energy for various GaAs and InP-based materials are given in Table 2.1 [26,27]. Enhancements in epitaxial growth techniques have enabled the possibility of growing lattice mismatched heterostructures [27]. In this situation, the lattice atoms change abruptly between the two semiconductor materials with dissimilar energy band gaps and lattice constants [24, 25]. This growth technique is known as *pseudomorphism* and will be discussed in the next section.

Table 2.1 Lattice constant and energy band gap of common III-V binary and ternary compound semiconductors at 300 K [26, 27]

Alloy	**Lattice constant, a_0 (Å)**	**Band gap, Eg (eV)**
GaAs	5.653	1.42
AlAs	5.660	2.16
InAs	6.058	0.37
InP	5.869	1.35
$In_{0.53}Ga_{0.47}As$	5.869	0.76
$In_{0.52}Al_{0.4}8As$	5.869	1.48

For an InP substrate, the lattice matched $In_{0.52}Al_{0.48}As$ is usually used as a buffer as it has a large band gap, resulting in improved insulation; and $In_{0.53}Ga_{0.47}As$ as a channel (due to its high mobility) followed by $In_{0.52}Al_{0.4}8As$ as a barrier (large ΔEc). Over the years, the state-of-art compound semiconductor technology has moved from GaAs channel (lattice constant =5.64Å) to $In_xGa_{1-x}As$/InP channels (5.87Å) which motivated by the higher saturation velocity in these materials [20].

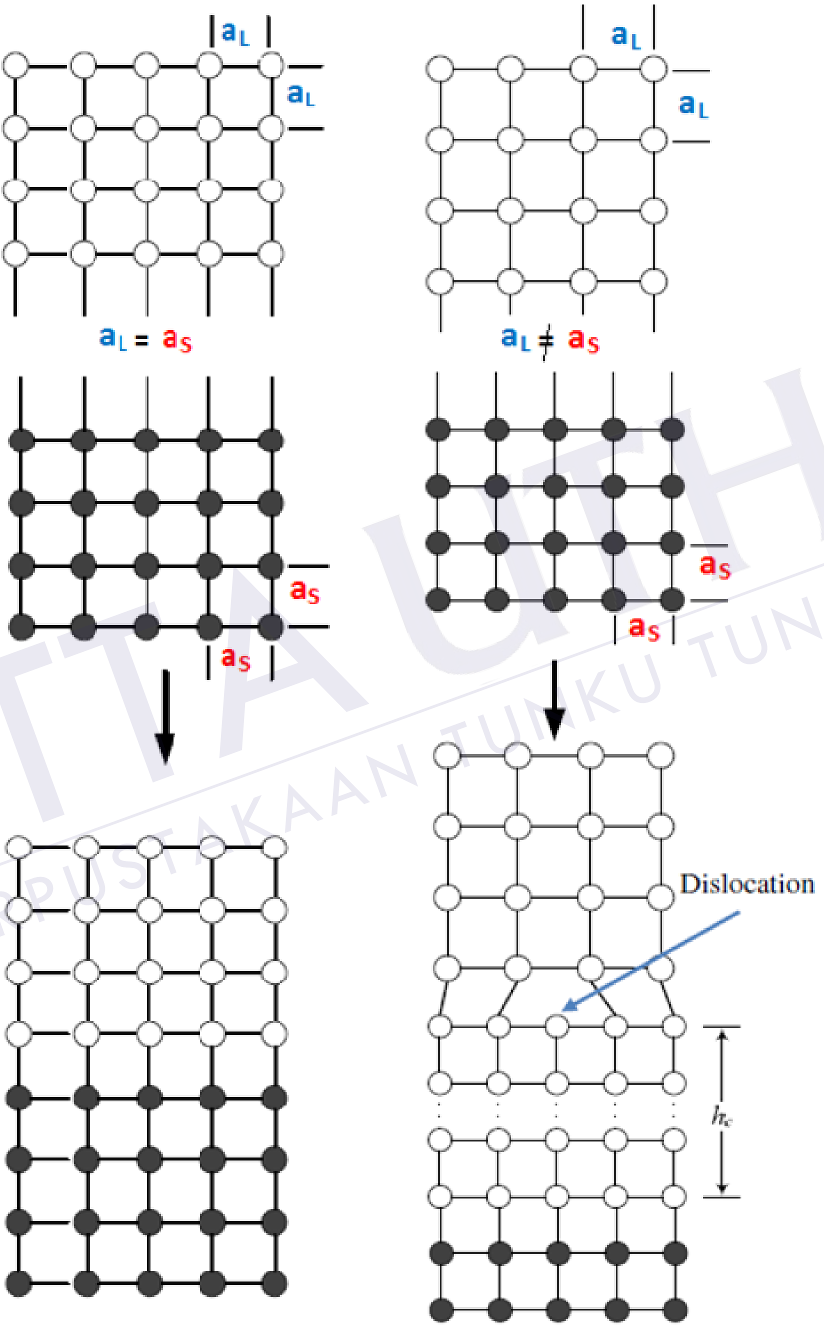
2.2.1 Lattice Matched and Pseudomorphic Material System

Ideally, heterostructures are formed by semiconductors with the same crystal structures and the same lattice constant. A HEMT structures grown with the same lattice constant are referred to as lattice matched HEMTs, i.e. $In_{0.53}Ga_{0.47}As$ and $In_{0.52}Al_{0.48}As$ (lattice matched to InP). Structures with slightly different lattice constant are known as Pseudomorphic HEMTs (pHEMTs). In modern epitaxial growth techniques, the thickness of lattice mismatched layers is kept within a certain critical thickness limit and the deposited layer must be very thin to avoid defect or dislocation formation [23, 29]. This new layer is called “pseudormorphic” as it alters its original crystal structure and physical properties, i.e., InGaAs-InAlAs, AlGaAs/InGaAs. For lattice mismatched, the atoms at the hetero-interface have to slightly adjust their positions in order for them to conserve the geometry of the lattice. The adjustments of the atomic position will result in a small strain at the interface. The critical thickness of grown epilayer (h_C) and the strain (ε) is given by Equation 2.22 and Equation 2.3. Respectively, a_S and a_L denotes the lattice constant for substrate and grown epilayer.

$$h_C = \frac{a_S}{2\varepsilon} \qquad \text{Equation 2.2}$$

$$\varepsilon = \frac{a_L - a_S}{a_S} \qquad \text{Equation 2.3}$$

The Figure 2.2 illustrates the crystal formation of the binary and ternary compound semiconductor material. In Figure 2.2 (a), a_L is in lattice matched with a_S, and hence the over-layer and base material atoms at the crystal interface are not required to adjust their positions relative to each other. However, lattice mismatched in the semiconductor may result in defects due to dislocations, as shown in Figure 2.2 (b). Above the critical thickness, the excessive strain energy is released by the formation of dislocations where some of the bonds are missing or extra bonds appear. These dislocations adversely affect the electrical characteristics of a device by creating localized states which act as traps for the charge carriers [29]. Materials that are not in lattice matched or have different inter-atomic lattice spacing are known as pseudomorphic i.e., AlGaAs and InGaAs. The formation of pseudomorphic crystal structure under compressive and tensile strains are shown in Figure 2.2 (c) and Figure 2.2 (d) respectively. When a_L is larger than a_S, the resultant relaxed material is under compressive strain whereas the atoms are under tensile strain when a_L is smaller than a_S.


aL
aL
aL = aS
aS
aS
aL
aL
aL ≠ aS
aS
aS
Dislocation
hc

(a) Lattice match

(b) Imperfect (dislocation)

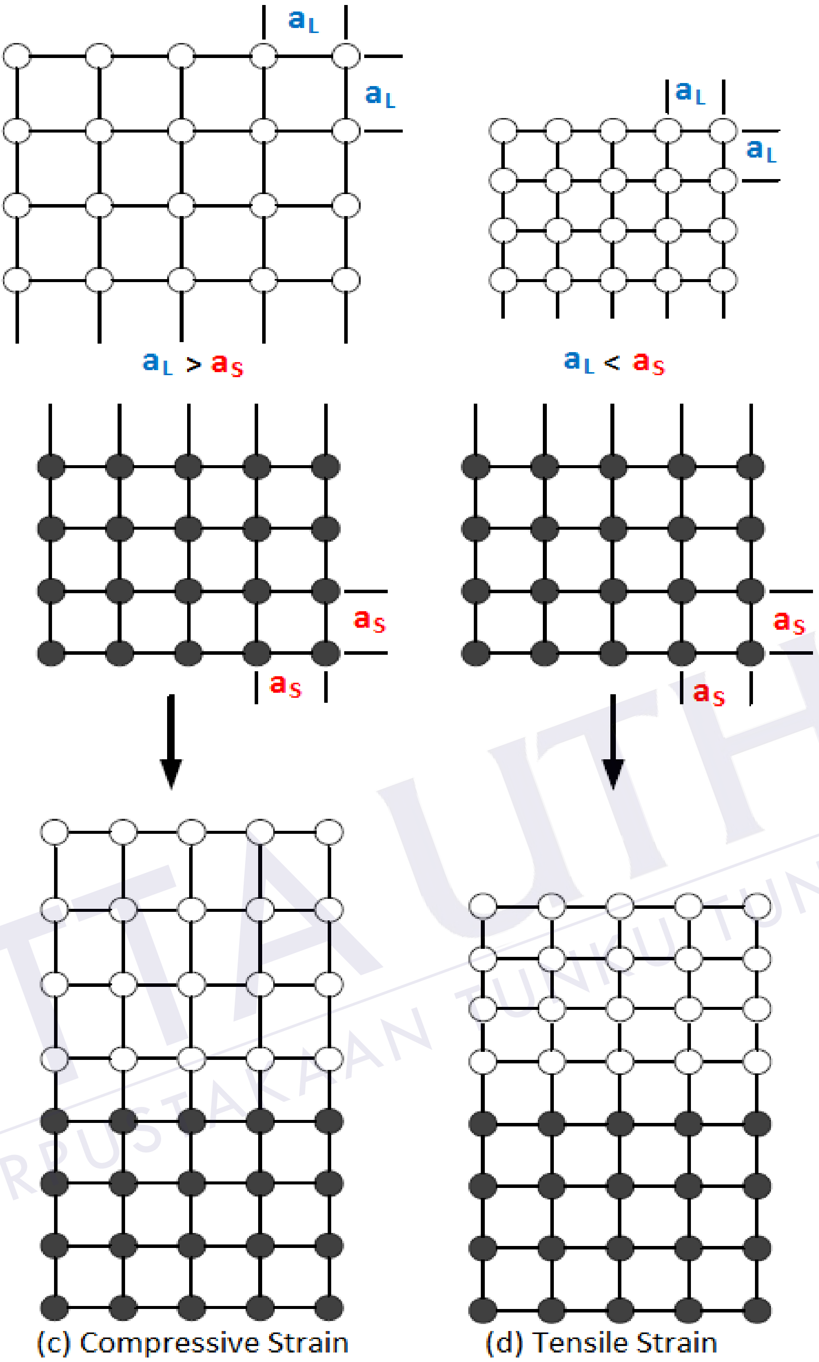
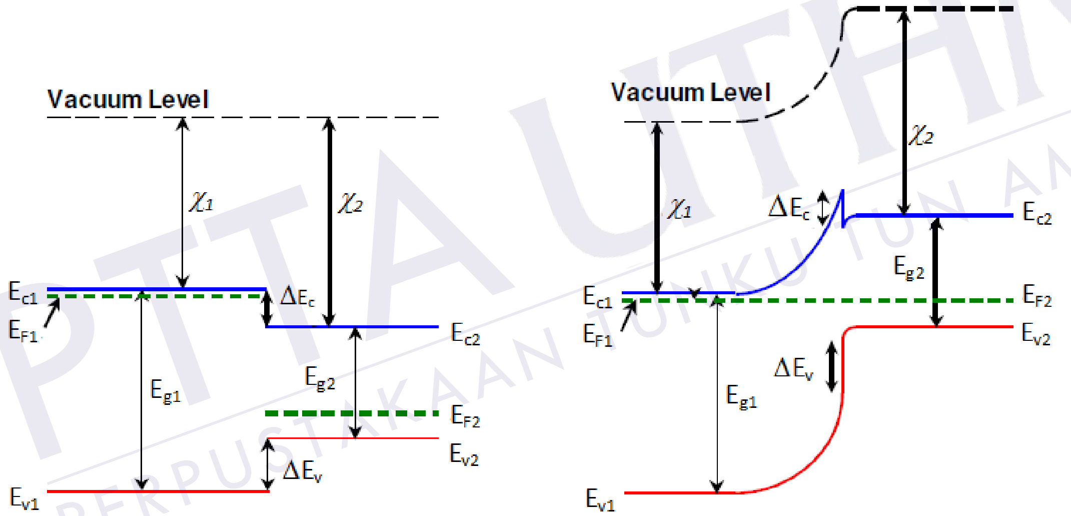

a_L
a_L
a_L
a_L
$a_L > a_S$
$a_L < a_S$
a_S
a_S
a_S
a_S
(c) Compressive Strain
(d) Tensile Strain

Figure 2.2 Conceptual formation of (a) lattice matched, (b) lattice mismatched with defects, and pseudormophic layers (c) Compressive and (d) Tensile strain

2.2.2 Band Discontinuity

Energy band discontinuity is the most important aspect of heterojunctions. It is an interesting features i.e., in HEMTs which can be used to modify the transport of charge carriers. The junction of two semiconductors with a difference in energy bandgaps results in an abrupt change in the energy band diagram of the heterostructure. Figure 2.3 shows the energy band diagram of two isolated semiconductors with the notation given by: E_C and E_V indicating conduction and valence bands, E_{g1} and E_{g2} the energy band gap for material A and material B, χ is the electron affinities, E_F is the Fermi level, ΔE_c the electron affinity, and ΔE_c and ΔE_v representing the conduction and valence band discontinuities between the two materials [33].


Vacuum Level
χ_1
χ_2
E_{c1}
E_{F1}
ΔE_c
E_{c2}
E_{g1}
E_{g2}
E_{F2}
E_{v2}
ΔE_v
E_{v1}
Vacuum Level
χ_2
χ_1
ΔE_c
E_{c2}
E_{g2}
E_{c1}
E_{F2}
E_{F1}
E_{v2}
ΔE_v
E_{g1}
E_{v1}

(a) (b)

Figure 2.3 Energy Band Diagrams for wide and narrow bandgap semiconductor (a) before and (b) after contact

The energy-band model of an ideal, abrupt heterojunction, was first established by Anderson [34]. The model assumes that ΔE_c was equal to the difference in electron affinities, χ as shown in Equation 2.4 and Equation 2.5.

$$\Delta E_c = \chi_1 - \chi_2$$

Equation 2.4

$$\Delta E_v = (E_{g2} - E_{g1}) - (\chi_1 - \chi_2)$$

Equation 2.5

Similarly, this could be written using Equation 2.6 and Equation 2.7,

$$\Delta E_g = E_{g1} - E_{g2} \qquad \text{Equation 2.6}$$

$$\Delta E_g = \Delta E_c + \Delta E_v \qquad \text{Equation 2.7}$$

In most semiconductors, the band gap engineering is very effective to attain numerous amounts of junction discontinuities. A larger band discontinuity, ΔE_C will lead to better carrier confinement and therefore a higher carrier concentration at the 2-DEG interface. The InAlAs/InGaAs/InP material system has many significant advantages over the AlGaAs/GaAs [24] or AlGaAs/InGaAs/GaAs material systems. The ΔE_C between $In_{0.52}Al_{0.48}As/In_{0.53}Ga_{0.47}As$ layer in InAlAs/InGaAs/InP material system (> 0.5eV) is higher than the ΔE_C between $Al_{0.2}Ga_{0.8}As/In_{0.15}Ga_{0.85}As$ layer (~ 0.3 eV) in the pseudomorphic AlGaAs/InGaAs/GaAs material system. The band discontinuity is even lower for $Al_{0.30}Ga_{0.70}As/GaAs$ hereterojunction where the ΔE_C is only 0.24 eV [16]. This property, therefore makes $In_{0.52}Al_{0.48}As/In_{0.53}Ga_{0.47}As/InP$ a prominent and suitable candidate for high-speed devices application with greater flexibility over carrier control at the junction.

2.2.3 Quantum Well and 2-DEG

When a thin layer of (~ 100 Å) of low band gap semiconductor material (e.g. GaAs) is sandwiched between two similar high band gap semiconductors (e.g. AlGaAs), a Quantum Well (QW) can be formed in the heterostructure. Such a heterojunction boundary will experience discontinuities at the edges of the conduction band and valence band with a QW generated for the carriers (electrons and holes) as illustrated in Figure 2.4. The dopants in the high band gap layers can supply the carriers to the quantum well. When the bottom of the quantum well is below the Fermi level, the high energy donors will go down to the well, hence creating a Two Dimensional Electron Gas (2DEG). This is shown in Figure 2.4 (c). The electron is free to move parallel to the interface, and so is quasi two-dimensional. However, the electrons in the quantum well is unable to move in the direction perpendicular to the interface, i.e. the crystal growth direction [35]. Careful choice of the materials and alloy compositions allow control of the carrier densities within the 2DEG.

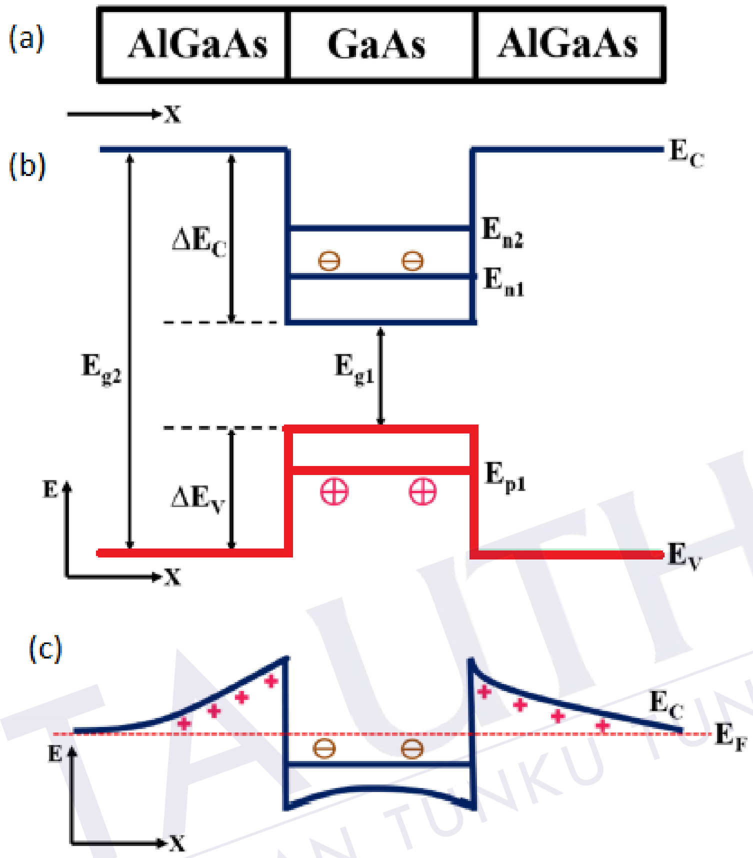

(a)
AlGaAs
GaAs
AlGaAs
X
(b)
ΔE_C
E_{g2}
E_{n2}
E_{n1}
E_{g1}
E_{p1}
ΔE_V
E_C
E_V
E
X
(c)
E_C
E_F
E
X

Figure 2.4 An ideal undoped square shape quantum well (a) Structure, Energy band diagram, and (c) Conduction band diagram if AlGaAs is n-doped [35]

2.3 Metal Semiconductor Contacts

Metal-semiconductor contacts are present in every semiconductor device. There are two types of contact for a metal-semiconductor junction; Schottky contact or ohmic contact depending on the nature of the interface. The details of these contacts are discussed in section 2.3.1 and section 2.3.2.

2.3.1 Ohmic Contact

An ohmic contact is formed if no potential barrier exists between the metal and semiconductor. It is a non-rectifying contact and does not control the flow of current, thus the current flows equally in both directions (reverse and forward) with linear I-V characteristic. On top of that, an ohmic contact should have an insignificant contact resistance, R_C relative to the series resistance, r_s of the semiconductor so that zero or very small current loss occurs across the device. There are 2 types of ohmic contact: (1) for n-type semiconductor; the metal workfunction, Φm must be closer to or smaller than the semiconductor electron affinity χ. Therefore, Φm must be smaller than the work-function of semiconductor Φs, i.e. Φs > Φm, as shown in Figure 2.5 (2) for a p-type semiconductor, Φm must be close to or larger than the sum of electron affinity and energy bandgap of the semiconductor, which is usually impractical. Hence p-type ohmic contacts are a lot more difficult to fabricate than n-type ones.

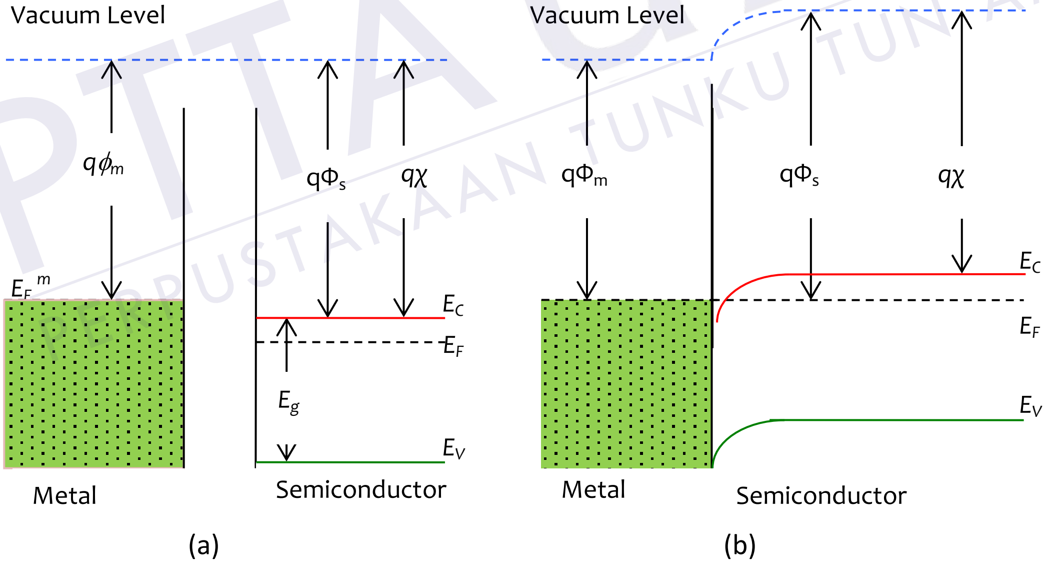
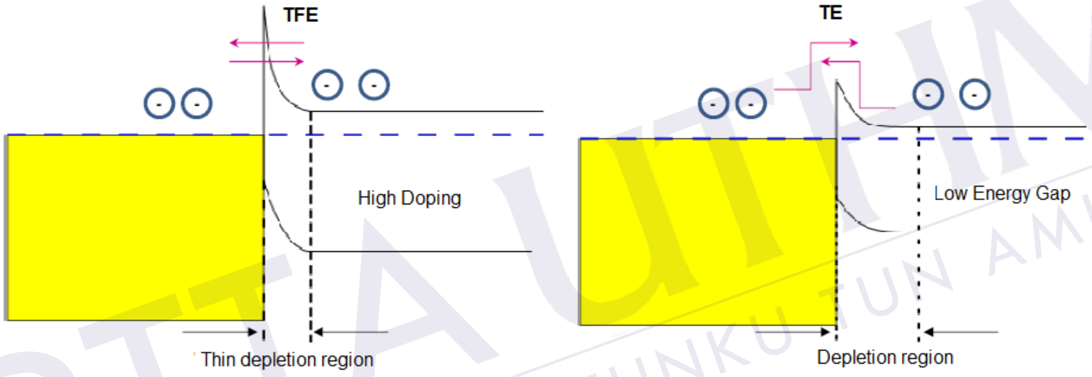


Figure 2.5 Band diagram of a metal-semiconductor interface:
(a) before contact and (b) after contact [33]

Practically, there are two ways in achieving a good ohmic contact in semiconductor processing: either by high semiconductor doping layer or through a low Schottky barrier height at metal-semiconductor junction. At any metal-semiconductor contact, there always exists a Schottky barrier [33]. The carriers must overcome this barrier in order to travel between the metal and semiconductor sides. When the semiconductor is heavily doped, i.e. $N_D \geq 10^{19}$ cm^{-3}, the depletion width and consequently the barrier width near the metal-semiconductor contact will be reduced. Electrons now can overcome this barrier and tunnel through it as the depletion width becomes sufficiently narrow. This mechanism is known as Thermionic Field Emission (TFE) [36]. Alternatively, the barrier height is reduced by means of a low energy gap material at the semiconductor side. Here, the electrons have energies larger than the potential barrier and Thermionic Emission (TE) takes place by electrons moving over the barrier [33]. Figure 2.6 illustrates the TFE and TE mechanism at the Schottky barrier interface.



(a) (b)

Figure 2.6 Current conduction at Ohmic contact (a) via TFE in highly doped semiconductor and (b) via TE at low Schottky barrier interface [33]

2.3.2 Schottky Contact

A Schottky contact (also known as rectifying contact), permits the flow of current in one direction and provides a barrier to the flow of current in the opposite direction. In Schottky contact, the semiconductor work-function, Φm is smaller than the work-function of the metal, Φm ($\Phi s < \Phi m$). Figure 2.7 (a) illustrates a metal to semiconductor interface before and after forming the Schottky contact for n-type semiconductor and metal contact. On contact, electrons from the semiconductor conduction band flow into lower energy states of metal, till a constant Fermi level is achieved at equilibrium condition. The flow of electrons will then leave a positive charge of ionised donor in the semiconductor which creates the depletion region of thickness, X_{dep} as illustrated in Figure 2.7 (b). The band bending at equilibrium, results in a potential barrier, Φ_b, at the interface and a built-in potential, V_{bi} that restricts further diffusion of electrons from semiconductor to metal. The exact shape of the conduction and valence bands is determined by solving the Schrödinger and Poisson equations self-consistently.

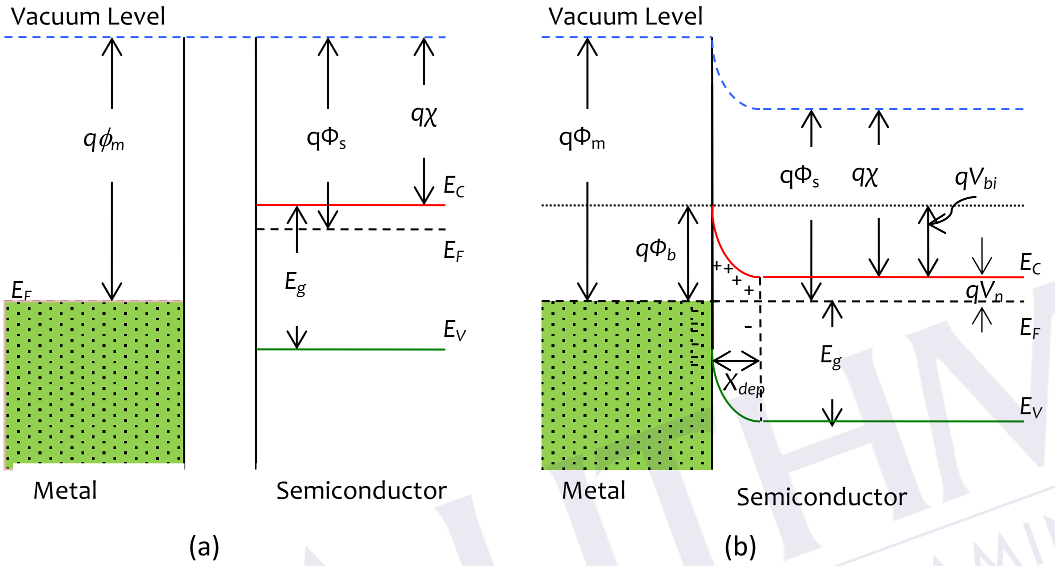

Vacuum Level
qϕm
qΦs
qχ
EC
EF
Eg
EV
EF
Metal
Semiconductor
(a)
Vacuum Level
qΦm
qΦs
qχ
qVbi
qΦb
EC
qVn
EF
Eg
Xdep
EV
Metal
Semiconductor
(b)

Figure 2.7 Energy and diagram of Schottky contact: (a) isolated and (b) on contact [33]

The built-in potential is given by Equation 2.8:

$$V_{bi} = \Phi_b - \Phi_n$$

Equation 2.8

where Φ_n is the potential difference between the minimum of conduction band (E_C) and Fermi level E_F, i.e.

$$\phi_n = \frac{E_C - E_F}{q}$$

Equation 2.9

The potential barrier, Φ_b, formed at the interface is related to the metal work-function, Φ_m and semiconductor electron affinity, χ_s as in Equation 2.10 and Equation 2.11:

$$\phi_B = \phi_m - \chi_s$$

Equation 2.10

$$\chi_S = \phi_S - \phi_n$$

Equation 2.11

Under zero bias condition, the net current flow between semiconductor to metal is zero because the same amount of current flows from semiconductor to metal and vice versa. However, under forward and reverse bias conditions, the flow of current transport changes due the changes in the V_{bi}. These conditions are illustrated in Figure 2.8 in which ϕ_B remains constant [12] in both figures.

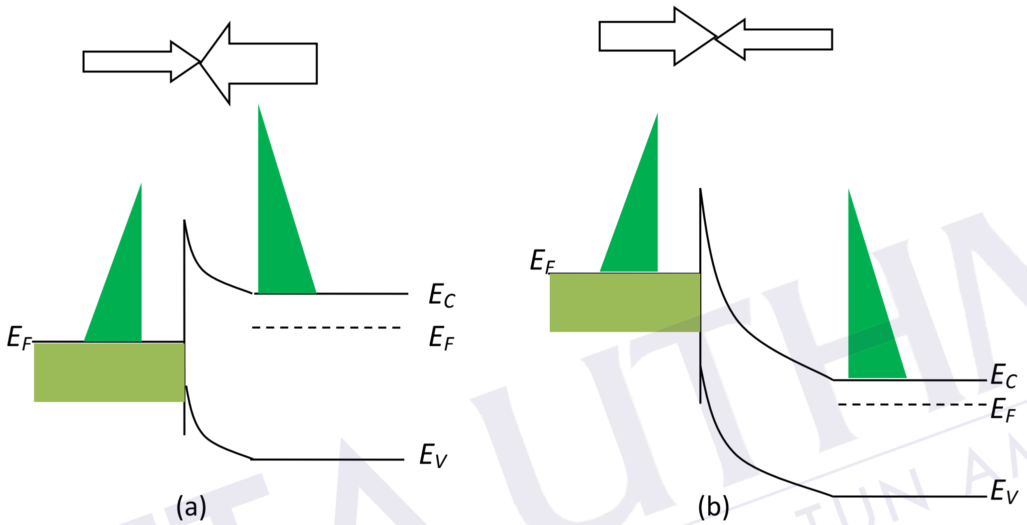
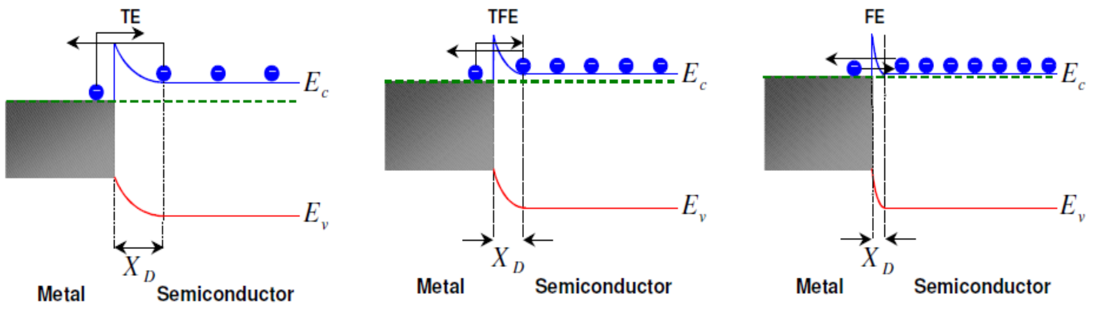


Figure 2.8 Current transport by thermionic emission in:
(a) forward bias and (b) reverse bias [33]

When a positive bias, e.g., V_F is applied to a metal, it will experience forward bias condition. Under this condition, the Fermi level, E_F will be shifted up and the built-in voltahe, V_{bi} will be reduced by a voltage V_F as illustrated in Figure 2.8 (a). The Figure 2.8 (b) shows that if a negative bias, i.e, $-V_R$ is applied to the metal, a reverse bias condition is achieved. In reversed bias condition, the Fermi level will be shifted down and the built-in-potential will increase by a voltage V_R. In a pHEMT, the quantity of electrons flow from metal to semiconductor under reverse bias condition is also known as leakage current [31]. The leakage current is one of the unwanted drawback for a pHEMT device which degrades its performance, particularly at high frequency applications.



(a)

Thermionic Emission (TE):
Carriers are thermally
excited over the barrier
(**Low N$_D$**)

(b)

Thermionic Field Emission
(TFE): Carriers are
thermally excited to an
energy where the barrier is
sufficiently narrow for the
tunneling to take place
(**Intermediate N$_D$**)

(c)

Field Emission (FE):
Carriers can tunnel through
entire barrier
(**High N$_D$**)

Figure 2.9 Depletion type contacts to n-type substrates with increasing doping concentration N_D: (a) Low N_D, (b) Intermediate N_D and (c) High N_D [37]

The mechanism of TE, TFE and FE at the barrier is shown in Figure 2.9. Theoretically, a metal with a higher Φ_m will yield a larger Schottky barrier on the same semiconductor. But this is not quite valid in practice. There is always an intermediate layer, contributing to the surface contamination of the metal or the surface states of the semiconductors such as native oxides or dangling bonds after etching, formed in between the metal and semiconductor. As a result, the Fermi level of a semiconductor will pin at the surface [38] of the intermediate layer before equilibrium is achieved. The resulting barrier height is not sensitive to the change of metal work function and such phenomenon is called Fermi-level pinning [33].

2.4 Introduction to High Electron Mobility Transistors (HEMTs)

HEMTs are very similar to Metal Semiconductor Field Effect Transistors (MESFET) in terms of structure and operations, but the key difference is the heterojunction structures. By bringing two dissimilar semiconductors to the junction, a potential well is formed in the channel due to the bending of energy level. This results in high density of carrier confinement in the well (channel), which only allows electron to move in a two-dimensional plane which creates the 2DEG layer. It is the high two-dimensional electron gas density with a high mobility and low scattering mechanism which contributes to naming the device the High Electron Mobility Transistor. This ultimately results in improved gain, noise and power performance of the device.

2.4.1 HEMT Epitaxial Layer

HEMT is a field effect transistor (FET) and utilises a vertical structure. A typical HEMT structure consists of epitaxial layers, namely cap layer, barrier layer, channel layer, and buffer layer which are grown on semi insulating substrates. These epilayer have different material parameters such as energy band gaps, doping concentration, layer thickness, etc. Figure 2.10 illustrates a conventional HEMT structure with a single delta doping layer.

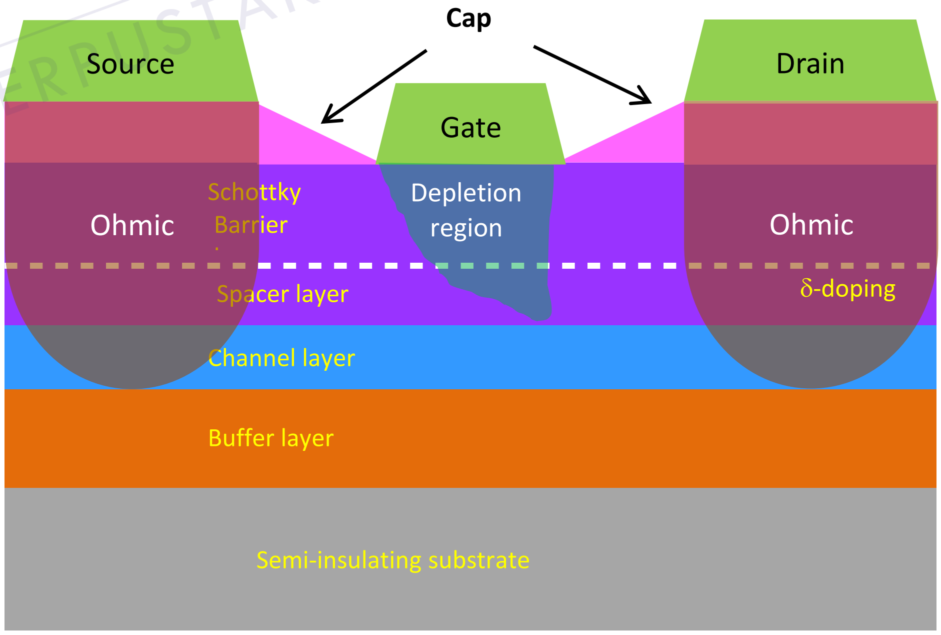


Figure 2.10 Cross section of conventional HEMT with δ-doped layer

2.4.1.1 Cap layer

The source and drain contacts are formed through the Cap layer. The Cap layer is heavily doped (usually >10^{18} cm^{-3}) to facilitate the formation of a low resistance for the source and drain metal contacts. The thickness of the cap layer is about 50Å to 100 Å [24]. Higher doping levels and a thicker capping layer would simultaneously reduce the device contact resistance [39] and effectively shorten the source-to-drain spacing; resulting in very high electron velocity, g_m, and f_T in the device. However, this also significantly reduces the device breakdown voltage, V_{BR}, and also increases the device output conductance, g_{ds}, and drain-to-gate feedback capacitance, C_{dg}. Another technique followed is the alloying and annealing technique in which electrons heavily diffuse down to the 2DEG thus reducing the potential barrier caused due to difference in electron concentration on both sides of the junction [35].

2.4.1.2 Supply Layer

The supply layer is formed beneath the cap Layer using a wide band gap material. Typically, the supply layer is uniformly doped with Si to supply carriers that diffuse into the channel and become available for conduction. The distance between gate and channel is very critical and is largely determined by the thickness of the supply layer [35]. A thinner supply layer allows for a small distance between the gate metal and the carrier channel that results in higher charge density in the channel, cutoff frequency,f_T and transconductance, g_m but reduces breakdown voltage. The thickness of supply layer and increasing doping concentration of the supply layer reduces the depletion width. If the depletion region is not fully formed, i.e. the supply layer is not fully depleted, poor field effect actions are expected to arise in this regime [40]. In order to eliminate parallel conduction in the supply layer, this layer must be completely depleted by both heterojunction and the Schottky gate.

2.4.1.3 Delta (δ) Doping Layer

A uniformly doped supply layer can be replaced by an undoped supply layer, followed by a very thin but extensively doped layer called a δ-doped layer (or pulse-doped). Hence, when the parallel conduction problem in the barrier layer is reduced, high sheet charge density and breakdown voltage can be achieved.

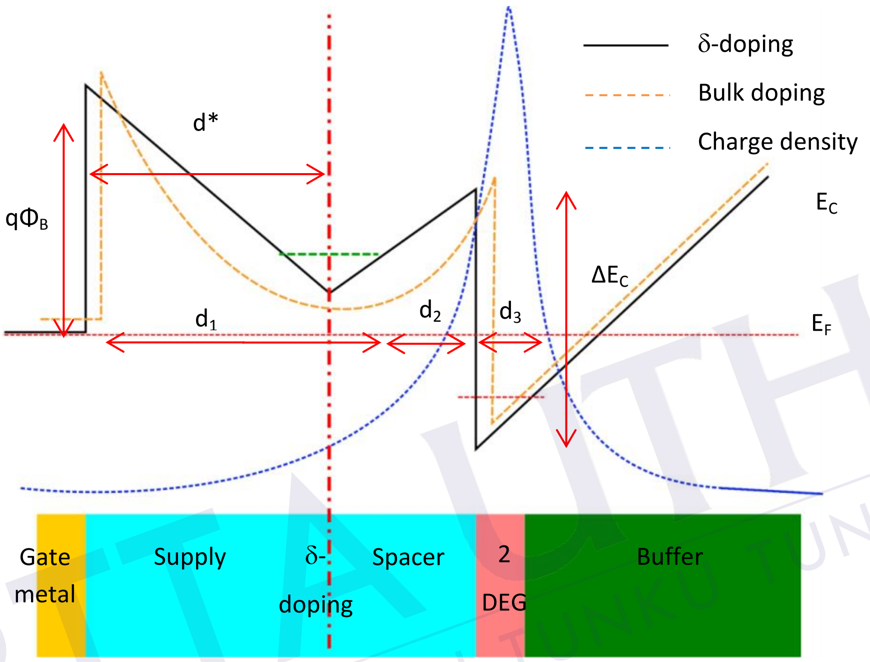


Figure 2.11 Conduction band of general depletion mode HEMT structure with δ-doping and bulk-doping [33]

As a result, the channel concentration increases. The difference of these doping to the structure is illustrated in Figure 2.11. The energy quantization occurs at the discontinuity formed between the high and low band gap materials. Electrons in the supply layer (bulk doping case) or δ-doping can then tunnel through the thin potential barrier and be trapped into the triangular QW. The electrons in the QW forms a high electron mobility plane called a 2DEG. The Coulomb scattering between electrons and the fixed ionized atoms separated by the spacer layer leads to high mobility. Figure 2.12 shows the relation of δ-doping concentration and the drain current as described in [41]. A degradation of the drain current is observed with reducing the δ-doping concentration.

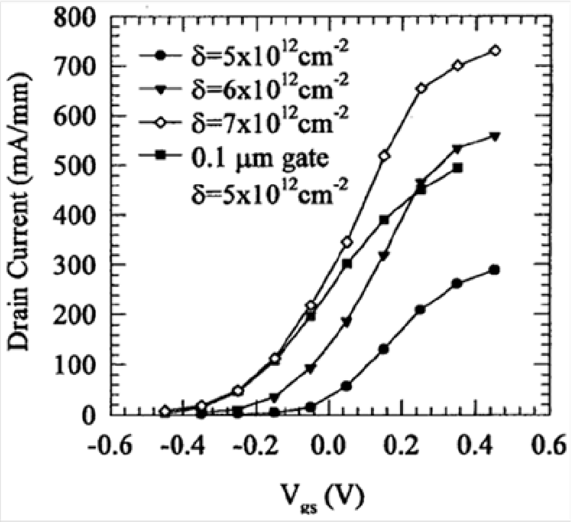


Figure 2.12 Drain Current versus δ-doping concentration variation [41]

2.4.1.4 Spacer Layer

A spacer layer of undoped materials i.e., AlGaAs or InAlAs is placed between the InAlAs donor and the InGaAs channel layer to separate the negatively charged 2DEG from the ionized dopant atoms. A thin spacer layer is preferred for low-noise and power devices due to the reduced parasitic source resistance and the increase in transconductance,g_m and current density. However, a thicker spacer layer might be applied to provide higher electron mobility with a smaller charge density in the channel. At cryogenic temperatures the noise performance of a HEMT is strongly dependent on the spacer thickness due to the large increase in electron mobility and velocity [6].

2.4.1.5 Channel Layer

The channel layer is a narrow bandgap undoped material, i.e. GaAs or InGaAs. These material systems improve transport properties due to the higher mobility of InGaAs and stronger electron confinement associated with the quantum well at the heterojunction. The barrier on both sides of the channel form heterojunctions on either edge of the channel layer thus building QW which confines high carrier concentration. These electrons have superior mobility characteristic because of high mobility and undoped nature of the channel material. Increasing the Indium concentration in the carrier channel of the pHEMT will result in further improvements in electron carrier confinement and transport properties [24].

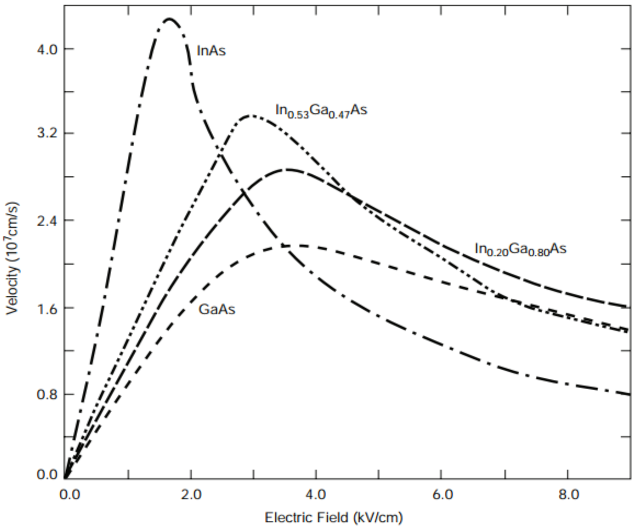


Figure 2.13 Electron velocity as a function of electric field for variety of Indium (In) concentrations of InGaAs [24].

For example, the performance of InP based pHEMT is directly related to the intrinsic properties of the InGaAs/InAlAs material system. The high indium content (typically 53 – 80%) InGaAs channel contributes to the high electron mobility and velocity [42]. Moreover, the large band discontinuities at the InGaAs/InAlAs heterojunctions will permit high two-dimensional electron gas (2DEG) densities. Figure 2.13 shows the electron velocity as a function of electric field for various In concentrations of InGaAs. Unfortunately, increasing the Indium concentration in $In_XGa_{1-X}As$ also increases the lattice constant [24].

2.4.1.6 Buffer Layer

Basically, the buffer layer is developed to confine the carriers to the device channel. It is also significant to isolate any unwanted defects on the substrate surface and also to de-couple it from the 2DEG [43]. The buffer layer is grown using undoped wide bandgap material that creates an energy barrier in the conduction band, thus reducing electron injection into the buffer or substrate. The electrons being injected into the substrate layer because of the application of Drain-to-Source electric field, contribute to the drain current, thus increasing the output conductance of the device and degrading the device pinch-off characteristic. The thick buffer layer is used to reduce any growth defects, and to accumulate any impurities from the substrate interface that may degrade the performance of the 2DEG channel [35].

REFERENCES

[1] R. L. Ross, S. P. Svensson, and P. Lugli, *Pseudomorphic HEMT Technology and Applications*. Springer Science & Business Media, 1996, p. 350.

[2] S. Silaj, M. T. Thahirally, and J. Wang, “Highly Linear LNA Design for 4G WiMAX Applications,” 2012.

[3] Y. Yamashita, A. Endoh, K. Shinohara, K. Hikosaka, T. Matsui, S. Hiyamizu, and T. Mimura, “Pseudomorphic In0.52Al0.48As/In0.7Ga0.3As HEMTs with an ultrahigh fT of 562 GHz,” *IEEE Electron Device Letters*, vol. 23, no. 10, 2002.

[4] D. H. Kim and J. A. del Alamo, “30-nm InAs pseudomorphic HEMTs on an InP substrate with a current-gain cutoff frequency of 628 GHz,” *IEEE Electron Device Letters*, vol. 29, pp. 830–833, 2008.

[5] D. Kim, “30-nm InAs PHEMTs With f T = 644 GHz and f max = 681 GHz,” *IEEE Electron Device Letters*, vol. 31, no. 8, pp. 806–808, 2010.

[6] D. S. Deakin, E. A. Sovero, and J. A. Higgins, “High-performance Ka-band monolithic low-noise amplifiers using 0.2-µm dry-recessed GaAs PHEMTs,” *IEEE Microwave and Guided Wave Letters*, vol. 6, no. 7, pp. 253–255, Jul. 1996.

[7] H. M. H. Morkner, M. F. M. Frank, and D. M. D. Millicker, “A high performance 1.5 dB low noise GaAss PHEMT MMIC amplifier for low cost 1.5-8 GHz commercial applications,” *IEEE 1993 Microwave and Millimeter-Wave Monolithic Circuits Symposium Digest of Papers*, 1993.

[8] A. de Boer, J. A. Hoogland, E. M. Suijker, M. van Wanum, and F. E. van Vliet, “Highly-Integrated X-band Multi-function MMIC with Integrated LNA and Driver Amplifier,” in *Gallium Arsenide Applications symposium. GAAS 2002*, 2002, pp. 6–9.

[9] D. Pavlidis, “HBT vs . PHEMT vs . MESFET : What ’ s best and why,” *International Conference on Compound Semiconductor Manufacturing Technology. 1999.*, pp. 1–4, 1999.

[10] Major G.P. Ohlke and M. G. J. Burton, “Millimeter Waves for Through-Wall Surveillance During Military Operations In Urban Terrain,” in *Technical report, Royal Military College of Canada, Kingston, Ontario, May 2004*.

[11] A. Bouloukou, A. Sobih, D. Kettle, J. Sly, and M. Missous, “Novel high-breakdown InGaAs/InAlAs pHEMTs for Radio Astronomy Applications,” *The 4th ESA Workshop on mm- Wave Technology and Applications*, 2006.

[12] D. Saguatti, M. M. Isa, K. W. Ian, A. Chini, G. Verzellesi, F. Fantini, and Mohamed Missous, “Improvement of Breakdown and DC-to-Pulse Dispersion Properties in Field-Plated InGaAs-InAlAs pHEMTs,” *23rd International Conference on Indium Phosphide and Related Materials - IPRM 2011*, pp. 22–24, 2011.

[13] B. Boudjelida, A. Sobih, A. Bouloukou, S. Boulay, S. Arshad, J. Sly, and M. Missous, “Modelling and simulation of low-frequency broadband LNA using InGaAs/InAlAs structures: A new approach,” *Materials Science in Semiconductor Processing*, vol. 11, no. 5–6, pp. 398–401, Oct. 2008.

[14] N. Ahmad, S. Arshad, and M. Missous, “New InP Based pHEMT Double Stage Differential to Single-ended MMIC Low Noise Amplifiers for SKA,” *The Eighth International Conference on Advanced Semiconductor Devices and Microsystems*, pp. 305–308, 2010.

[15] I. Ingaas, M. H. Somerville, A. Ernst, J. A. Alamo, and S. Member, “A Physical Model for the Kink Effect in,” vol. 47, no. 5, pp. 922–930, 2000.

[16] M. Gassoumi, J. M. Bluet, C. Gaquière, G. Guillot, and H. Maaref, “Deep levels and nonlinear characterization of AlGaN/GaN HEMTs on silicon carbide substrate,” *Microelectronics Journal*, vol. 40, no. 8, pp. 1161–1165, Aug. 2009.

[17] I. Angelov, H. Zirath, and N. Rosman, “A new empirical nonlinear model for HEMT and MESFET devices,” *IEEE Transactions on Microwave Theory and Techniques*, vol. 40, 1992.

[18] G. Dambrine, A. Cappy, F. Heliodore, and E. Playez, “A new method for determining the FET small-signal equivalent circuit,” *IEEE Transactions on Microwave Theory and Techniques*, vol. 36, no. 7, pp. 1151–1159, Jul. 1988.

[19] D. Donoval, A. Vrbicky, A. Chvala, and P. Beno, *Transistor Level Modeling for Analog/RF IC Design*. Dordrecht: Springer Netherlands, 2006, pp. 1–27.

[20] D. Hoare and R. a. Abram, “Monte Carlo simulation of PHEMTs operating up to terahertz frequencies,” *International Journal of Electronics*, vol. 83, no. 4, pp. 429–440, Oct. 1997.

[21] T. Watanabe, K. Akagawa, Y. Tanimoto, D. Coquillat, W. Knap, and T. Otsuji, “Terahertz Imaging with InP High-electron-mobility Transistors,” in *Proceedings of SPIE - The International Society for Optical Engineering*, 2011, p. 80230P–80230P–6.

[22] P. E. Dewdney and T. J. Lazio, “The square kilometer array (SKA) radio telescope: Progress and technical directions,” *Radio Science Bulletin*, vol. no. 326, p. p. 5, 2008.

[23] J. A. del Alamo, “Nanometre-scale electronics with III–V compound semiconductors,” *Nature*, vol. 479. pp. 317–323, 2011.

[24] J. Javier Bautista, “Chapter 5 HEMT Low-Noise Amplifiers,” in *Low-Noise Systems in the Deep Space Network*, Macgregor S. Reid, Ed. 2008, pp. 195–243.

[25] L. De Caro, C. Giannini, L. Tapfer, H.-P. Schönherr, L. Däweritz, and K. H. Ploog, “Validity of vegard’s rule for the lattice parameter and the stiffness elastic constant ratios of the AlGaAs ternary compound,” *Solid State Communications*, vol. 108. pp. 599–603, 1998.

[26] J. C. Mikkelsen and J. B. Boyce, “Atomic-Scale Structure of Random Solid Solutions: Extended X-Ray-Absorption Fine-Structure Study of Ga 1 − x In x As,” *Physical Review Letters*, vol. 49, no. 19, pp. 1412–1415, Nov. 1982.

[27] T. F. Kuech, S. Jha, T. S. Kuan, S. E. Babcock, and L. J. Mawst, “Defect reduction in large lattice mismatch epitaxial growth through block copolymer full wafer patterning,” in *2009 IEEE International Conference on Indium Phosphide & Related Materials*, 2009, pp. 63–64.

[28] J. W. Matthews, “Defects in epitaxial multilayers II. Dislocation pile-ups, threading dislocations, slip lines and cracks,” *Journal of Crystal Growth*, vol. 29, no. 3, pp. 273–280, Jul. 1975.

[29] J. W. Matthews and A. E. Blakeslee, “Defects in epitaxial multilayers: I. Misfit dislocations,” *Journal of Crystal Growth*, vol. 27, no. 2, pp. 118–125, Feb. 1974.

[30] B.Jalali and S.Pearton, *InP HBTs: growth, processing, and applications*. Artech House Publishers, 1995.

[31] W. R. Frensley and N. G. Einspruch, “Heterostructures and Quantum Devices,” *VLSI Electronics: Microstructure Science, ed San Diego:Academic Press, 1995.*, Jan. 1994.

[32] G. Bauer and F. Schäffler, “Self-assembled Si and SiGe nanostructures: New growth concepts and structural analysis,” *physica status solidi (a)*, vol. 203, no. 14, pp. 3496–3505, Nov. 2006.

[33] S. M. Sze and K. K. Ng, *Physics of Semiconductor Devices*, vol. 3. John Wiley & Sons, 2006, p. 832.

[34] R. L. Anderson, “Experiments on Ge-GaAs heterojunctions,” *Solid-State Electronics*, vol. 5, no. 5, pp. 341–351, Sep. 1962.

[35] M. Missous., “Ultra High Speed Nanoelectronics Devices [Lecture hand out].” [Online]. Available: http://intranet.eee.manchester.ac.uk/intranet/pg/coursematerial/MSc Co.

[36] F. A. Padovani and R. Stratton, “Field and thermionic-field emission in Schottky barriers,” *Solid-State Electronics*, vol. 9, no. 7, pp. 695–707, Jul. 1966.

[37] J. d. F. Sexton, “Fabrication and Characterisation of High-Speed Indium Phosphide-Based Heterojunction Bipolar Transistors,” PhD Thesis, The University of Manchester, 2005.

[38] M. H. Somerville, A. Ernst, J. A. Alamo, and S. Member, “A Physical Model for the Kink Effect in InAlAs/InGaAs HEMT’s,” *IEEE Transactions on Electron Devices*, vol. 47, no. 5, pp. 922–930, 2000.

[39] B.-U. H. Klepser, C. Bergamaschi, and W. Patrick, “Influence of cap-layer doping on ohmic contacts for InP based HEMT structures,” *Solid-State Electronics*, vol. 37, no. 12, pp. 1905–1906, Dec. 1994.

[40] “What is a HEMT | High Electron Mobility Transistor / HFET / MODFET | Tutorial.” [Online]. Available: http://www.radio-electronics.com/info/data/semicond/fet-field-effect-transistor/hemt-phemt-transistor.php. [Accessed: 12-Apr-2015].

[41] T. Parenty, S. Bollaert, and J. Mateos, “Design and realization of sub 100nm gate length,” *2001 International Conference on Indium Phosphide and Related Materials*, no. May, pp. 626–629, 2001.

[42] P. M. Smith, “Status of InP HEMT technology for microwave receiver applications,” *IEEE Transactions on Microwave Theory and Techniques*, vol. 44, no. 12, pp. 2328–2333, 1996.

[43] I. D. Robertson, S. Lucyszyn, and I. of E. Engineers, *RFIC and MMIC Design and Technology*. IET, 2001, p. 562.

[44] K. Kalna and a. Asenov, “Role of multiple delta doping in PHEMTs scaled to sub-100 nm dimensions,” *Solid-State Electronics*, vol. 48, no. 7, pp. 1223–1232, Jul. 2004.

[45] T. Suemitsu, T. Enoki, and N. Sano, “An Analysis of the Kink Phenomena in InAlAs / InGaAs HEMT ’ s Using Two-Dimensional Device Simulation,” *IEEE Transactions on Electron Devices*, vol. 45, no. 12, pp. 2390–2399, 1998.

[46] R. Lai, X. B. Mei, W. R. Deal, W. Yoshida, Y. M. Kim, P. H. Liu, J. Lee, J. Uyeda, V. Radisic, M. Lange, T. Gaier, L. Samoska, and A. Fung, “Sub 50 nm InP HEMT Device with Fmax Greater than 1 THz,” in *2007 IEEE International Electron Devices Meeting*, 2007, pp. 609–611.

[47] A. Bouloukou, B. Boudjelida, A. Sobih, S. Boulay, J. Sly, and M. Missous, “Very low leakage InGaAs/InAlAs pHEMTs for broadband (300 MHz to 2 GHz) low-noise applications,” *Materials Science in Semiconductor Processing*, vol. 11, pp. 390–393, 2008.

[48] Y.-W. Chen, W.-C. Hsu, R.-T. Hsu, Y.-H. Wu, and Y.-J. Chen, “Characteristics of In0.52Al0.48As/InxGa1−xAs HEMT’s with various InxGa1−xAs channels,” *Solid-State Electronics*, vol. 48, no. 1, pp. 119–124, Jan. 2004.

[49] J. A. del Alamo and J. Joh, “GaN HEMT reliability,” *Microelectronics Reliability*, vol. 49, pp. 1200–1206, 2009.

[50] H. Yoon, J. Lee, B. Park, C. Yun, and C. Park, “Fabrication and Characteristics of Extremely Low-Noise AlGaAs / InGaAs / GaAs Pseudomorphic HEMTs,” *Journal of the Korean Physical Society*, vol. 33, no. 6, pp. 741–744, 1998.

[51] H. T. Kim and D. M. Kim., “Electrical Characteristics of InAlAs/InGaAs/InAlAs Pseudomorphic High Electron Mobility Transistors under Sub-Bandgap Photonic Excitation,” *JOURNAL OF SEMICONDUCTOR TECHNOLOGY AND SCIENCE 3.3 (2003): 145*.

[52] T. Suemitsu, H. Yokoyama, T. Ishii, T. Enoki, G. Meneghesso, and E. Zanoni, “30-nm two-step recess gate InP-based InAlAs/InGaAs HEMTs,” *IEEE Transactions on Electron Devices*, vol. 49, pp. 1694–1700, 2002.

[53] R. Gupta, S. K. Aggarwal, M. Gupta, and R. S. Gupta, “Analytical non-linear charge control model for InAlAs/InGaAs/InAlAs double heterostructure high electron mobility transistor (DH-HEMT),” *Solid-State Electronics*, vol. 49, pp. 167–174, 2005.

[54] D.Théron et.al, “HEMT Structures and Technology on GaAs and InP for Power Amplification in Millimetre Wave Range,” *Gallium Arsenide applications symposium. Gaas 2001*, 2001.

[55] K. Kalna, K. Elgaid, I. Thayne, and A. Asenov, “MODELLING OF INP HEMTS WITH HIGH INDIUM CONTENT CHANNELS,” *2005 International Conference in Indium Phosphide and Related Materials*, pp. 192–195, 2005.

[56] K. Kalna and A. Asenov, “Tunnelling and impact ionization in scaled double doped PHEMTs,” no. Mc, pp. 2–5.

[57] S. Long, L. Escotte, J. Graffeuill, P. Fellon, D. Roques, L. Cnfs, P. Sabatier, and C. Roche, “Ka-band Coplanar Low-Noise Amplifier Design with Power PHEMTs,” *33rd European Microwave Conference*, vol. 33, no. 0, pp. 31–34, 2003.

[58] Y. Awano, M. Kosugi, K. Kosemura, and T. Mimura, “Short-Channel Effects in Subquarter-Micrometer-Gate HEMT ’ s : Simulation and Experiment,” *IEEE Transactions on Electron Devices*, vol. 36, no. 10, pp. 2260–2266, 1989.

[59] G. I. Ng, K. Radhakrishnan, and H. Wang, “Are we there yet? - a metamorphic HEMT and HBT perspective,” in *Gallium Arsenide and Other Semiconductor Application Symposium, 2005. EGAAS 2005. European*, 2005, pp. 13–19.

[60] B. G. Vasallo, J. Mateos, D. Pardo, and T. González, “Influence of the kink effect on the dynamic performance of short-channel InAlAs/InGaAs high electron mobility transistors,” *Semiconductor Science and Technology*, vol. 20, no. 9, pp. 956–960, Sep. 2005.

[61] W.Shockley, “Circuit element utilizing semiconductive material,” U. S. Patent 256934725-Sep-1951.

[62] R. Dingle, H. L. Störmer, A. C. Gossard, and W. Wiegmann, “Electron mobilities in modulation-doped semiconductor heterojunction superlattices,” *Applied Physics Letters*, vol. 33, no. 7, p. 665, Aug. 1978.

[63] A.Y.Cho, “Morphology of Epitaxial Growth of GaAs by a Molecular Beam Method: The Observation of Surface Structures,” *Journal of Applied Physics*, vol. 41, no. 7, p. 2780, 1970.

[64] J. R. Arthur, “GaAs, GaP, and GaAs[sub x]P[sub 1−x] Epitaxial Films Grown by Molecular Beam Deposition,” *Journal of Vacuum Science and Technology*, vol. 6, no. 4, p. 545, Jul. 1969.

[65] T. Mimura and S. Hiyamizu, “A new field-effect transistor with selectively doped GaAs/n-AlxGa1-xAs heterojunctions,” *Japanese journal of …*, vol. 225, 1980.

[66] L. Esaki and R. Tsu, “Superlattice and Negative Differential Conductivity in Semiconductors,” *IBM Journal of Research and Development*, vol. 14, no. 1, pp. 61–65, Jan. 1970.

[67] H. L. S. R. Dingle, Arthur C. Gossard, “High mobility multilayered heterojunction devices employing modulated doping,” 416323731-Jul-1979.

[68] H. Morkoc, “Current transport in modulation doped (Al, Ga) As/GaAs heterostructures: Applications to high speed FET’s,” *Electron Device Letters, IEEE*, no. 10, pp. 260–262, 1981.

[69] T. E. Zipperian and T. J. Drummond, “Strained-quantum-well, modulation-doped, field-effect transistor,” *Electronics Letters vol. 21 (18) p. 823*, vol. 21, no. 18, p. 823, 1985.

[70] J. J. Rosenberg, M. Benlamri, P. D. Kirchner, J. M. Woodall, and G. D. Pettit, “An In<inf>0.15</inf>Ga<inf>0.85</inf>As/GaAs pseudomorphic single quantum well HEMT,” *IEEE Electron Device Letters vol. 6 (10) p. 491-493*, vol. 6, no. 10, pp. 491–493, Oct. 1985.

[71] A. Ketterson, M. Moloney, W. T. Masselink, C. K. Peng, J. Klem, R. Fischer, W. Kopp, and H. Morkoc, “High transconductance InGaAs/AlGaAs pseudomorphic modulation-doped field-effect transistors,” *IEEE Electron Device Letters vol. 6 (12) p. 628-630*, vol. 6, no. 12, pp. 628–630, Dec. 1985.

[72] N. Moll, A. Fischer-Colbrie, and M. Hueschen, “IIA-5 Pulse-doped AlGaAs/InGaAs pseudomorphic MODFET’s,” *IEEE Transactions on Electron Devices vol. 34 (11) p. 2357-2358*, vol. 34, no. 11, pp. 2357–2358, Nov. 1987.

[73] U. K. Mishra, A. S. Brown, and S. E. Rosenbaum, “DC and RF performance of 0.1 mu m gate length Al/sub 0.48/In/sub 0.52/As-Ga/sub 0.38/In/sub 0.62/As

pseudomorphic HEMTs," in *Technical Digest., International Electron Devices Meeting p. 180-183*, 1988, pp. 180–183.

[74] M. Aust, J. Yonaki, K. Nakano, J. Berenz, G. S. Dow, and L. C. T. Liu, "A family of InGaAs/AlGaAs V-band monolithic HEMT LNAs," in *11th Annual Gallium Arsenide Integrated Circuit (GaAs IC) Symposium*, 1989, pp. 95–98.

[75] M. C. Foisy, P. J. Tasker, B. Hughes, and L. F. Eastman, "The role of inefficient charge modulations in limiting the current-gain cutoff frequency of the MODFET," *IEEE Transactions on Electron Devices vol. 35 (7) p. 871-878*, vol. 35, no. 7, pp. 871–878, Jul. 1988.

[76] Z. Hamaizia, N. Sengouga, M. Missous, and M. C. E. Yagoub, "A 0.4dB noise figure wideband low-noise amplifier using a novel InGaAs/InAlAs/InP device," *Materials Science in Semiconductor Processing*, vol. 14, no. 2, pp. 89–93, Jun. 2011.

[77] E. F. Schubert, A. Fischer, and K. Ploog, "The delta-doped field-effect transistor (&#948;FET)," *IEEE Transactions on Electron Devices*, vol. 33, no. 5, pp. 625–632, May 1986.

[78] T. Simlinger, H. Brech, T. Grave, and S. Selberherr, "Simulation of Submicron Double- Heterojunction High Electron Mobility Transistors with MINIMOS-NT," vol. 44, no. 5, pp. 700–707, 1997.

[79] A. Asgari, M. Karamad, and M. Kalafi, "Modeling of trap-assisted tunneling in AlGaN/GaN heterostructure field effect transistors with different Al mole fractions," *Superlattices and Microstructures*, vol. 40, no. 4–6, pp. 603–606, Oct. 2006.

[80] Silvaco Inc., "ATLAS User ' s Manual," no. 408, pp. 567–1000, 2010.

[81] B. G. Vasallo, J. Mateos, D. Pardo, and T. González, "Monte Carlo study of kink effect in short-channel InAlAs/InGaAs high electron mobility transistors," *Journal of Applied Physics*, vol. 94, no. 6, p. 4096, 2003.

[82] N. J. Pilgrim, W. Batty, and R. W. Kelsall, "Electrothermal Monte Carlo Simulations of InGaAs / AlGaAs HEMTs," pp. 207–211, 2003.

[83] V. Palankovski and R. Quay, *Analysis and Simulation of Heterostructure Devices*. Vienna: Springer Vienna, 2004.

[84] S. Arshad, M. Mohiuddin, A. Bouloukou, and M. Missous, "Physical Modelling of the Kink Effect in Strained InGaAs / InAlAs pHEMTs," *ASDAM 2008 - Conference Proceedings of the 7th International Conference on Advanced Semiconductor Devices and Microsystems*, pp. 55–58, 2008.

[85] R. T. Webster, S. Wu, and A. F. M. Anwar, "Impact Ionization in InAlAs / InGaAs / InAlAs HEMT ' s," *IEEE Electron Device Letters*, vol. 21, no. 5, pp. 193–195, 2000.

[86] A. Mazzanti, G. Verzellesi, C. Canali, G. Meneghesso, E. Zanoni, and S. Member, "Physics-Based Explanation of Kink Dynamics in AlGaAs / GaAs HFETs," *IEEE Electron Device Letters*, vol. 23, no. 7, pp. 383–385, 2002.

[87] S. Rathi, J. Jogi, M. Gupta, and R. S. Gupta, "An analytical charge-based drain current model for nano-scale In 0.52 Al 0.48 As–In 0.53 Ga 0.47 as a separated double-gate HEMT," *Semiconductor Science and Technology*, vol. 25, no. 11, p. 115003, Nov. 2010.

[88] S. Selberherr, "Process and device modeling for VISI," *Microelectronics Reliability*, vol. 24, no. 2, pp. 225–257, Jan. 1984.

[89] M. Mohiuddin, S. Arshad, A. Bouloukou, and M. Missous, "2-D Physical Modelling of delta-doped GaAs/AlGaAs HEMT," in *2008 International Conference on Advanced Semiconductor Devices and Microsystems*, 2008, pp. 207–210.

[90] J. G. Rathmell and A. E. Parker, "Circuit Implementation of a Theoretical Model of Trap Centres in GaAs and GaN Devices," *Proceedings of SPIE - The International Society for Optical Engineering*, 2007.

[91] E. W. Faraclas and a. F. M. Anwar, "AlGaN/GaN HEMTs: Experiment and simulation of DC characteristics," *Solid-State Electronics*, vol. 50, no. 6, pp. 1051–1056, Jun. 2006.

[92] M. Charfeddine, F. Echouchene, H. Mosbahi, M. A. Zaidi, and H. Maaref, “Theoretical Investigation of Kink Effect and Deep Defects in AlGaN / GaN HEMTs,” vol. x, pp. 1–8.

[93] R. Singh and C. M. Snowden, “A charge-control HEMT model incorporating deep level effects,” *Solid-State Electronics*, vol. 43, no. 3, pp. 473–480, Mar. 1999.

[94] J. G. Rathmell and A. E. Parker, “Circuit Implementation of a Theoretical Model of Trap Centres in GaAs and GaN Devices,” 2006.

[95] Norhawati Ahmad, “Modelling and Design of Low Noise Amplifiers Using Strained InGaAs/InALAs/InP pHEMT For the Square Kilometre Array (SKA) Application,” The University of Manchester, 2012.

[96] Muammar Mohamad Isa, “Low Noise Amplifiers Using Highly Strained InGaAs/InAlAs/InP pHEMT For Implementation In The Square Kilometre Array (SKA),” The University of Manchester, 2012.

[97] K. W. Ian and M. Missous, “Thermally stable In 0.7 Ga 0.3 As/In 0.52 Al 0.48 As pHEMTs using thermally evaporated palladium gate metallization,” *Semiconductor Science and Technology*, vol. 29, no. 3, p. 035009, Mar. 2014.

[98] Ka Wa Ian, “ROUTES TO COST EFFECTIVE RELISATION OF HIGH PERFORMANCE SUBMICRON GATE InGaAs/InAlAs/InP pHEMT,” The University of Manchester, 2013.

[99] K. W. Ian, M. Exarchos, and M. Missous, “Fabrication of 250-nm T-gate In<inf>52</inf>Al<inf>48</inf>As-In<inf>70</inf>Ga<inf>30</inf>As pHEMT using a novel solvent reflow technique at room temperature,” in *The Ninth International Conference on Advanced Semiconductor Devices and Mircosystems*, 2012, pp. 99–102.

[100] H.-C. Chiu, C.-W. Yang, C.-H. Chen, C.-K. Lin, J. S. Fu, H.-Y. Tu, and S.-F. Tang, “High thermal stability AlGaAs/InGaAs enhancement-mode pHEMT using palladium-gate technology,” *Microelectronics Reliability*, vol. 50, no. 6, pp. 847–850, Jun. 2010.

[101] T. Ishikura, Z. Cui, T. Matsuda, and K. Yoh, “Thermal Stability of Pd Gate in Pseudomorphic InGaAs Heterostructures,” *Japanese Journal of Applied Physics*, vol. 50, no. 6, p. 06GF19, Jun. 2011.

[102] R. Gupta, S. Rathi, R. Kaur, M. Gupta, and R. S. Gupta, “T-gate geometric (solution for submicrometer gate length) HEMT: Physical analysis, modeling and implementation as parasitic elements and its usage as dual gate for variable gain amplifiers,” *Superlattices and Microstructures*, vol. 45, no. 3, pp. 105–116, Mar. 2009.

[103] L. D. Nguyen, M. V. Le, T. Liu, M. Lui, K. Kaneko, E. Holzman, and M. J. Delaney, “Millimeter wave InP HEMT technology: Performance and applications,” in *Solid-State Electronics*, 1995, vol. 38, pp. 1575–1579.

[104] S.M.Sze, *SEMICONDUCTOR DEVICES: PHYSICS AND TECHNOLOGY, 2ND ED*. Wiley India Pvt. Limited, 2008, p. 572.

[105] Angeliki Bouloukou, “Novel, High-breakdown, Low-Noise InGaAs-InAlAs Transistors for Radio Astronomy Applications,” The University of Manchester, 2006.

[106] A. Asgari, M. Kalafi, and L. Faraone, “The effects of GaN capping layer thickness on two-dimensional electron mobility in GaN/AlGaN/GaN heterostructures,” *Physica E: Low-dimensional Systems and Nanostructures*, vol. 25, no. 4, pp. 431–437, Jan. 2005.

[107] T. Baksht, S. Member, S. Solodky, M. Leibovitch, and G. Bunin, “Impact Ionization Measurements and Modeling for Power PHEMT,” *IEEE Transactions on Electron Devices*, vol. 50, no. 2, pp. 479–485, 2003.

[108] K. KaIna, K. Elgaid, I. Thayne, and A. Asenov, “Modelling of InP HEMTs with high indium content channels,” in *International Conference on Indium Phosphide and Related Materials, 2005.*, 2005, pp. 192–195.

[109] J. M. Dumas, P. Audren, M. P. Favennec, D. Lecrosnier, S. R. Bahl, and J. A. del Alamo, “An investigation of deep levels in InAlAs/n/sup +/-InGaAs heterostructure

FETs," in *1993 (5th) International Conference on Indium Phosphide and Related Materials*, 1993, pp. 255–258.

[110] S. Arshad, "LOW NOISE AMPLIFIERS FOR THE SQUARE KILOMETRE ARRAY RADIO TELESCOPE," University of Manchester, 2009.

[111] M. Charfeddine, H. Belmabrouk, M. A. Zaidi, and H. Maaref, "2-D Theoretical Model for Current-Voltage Characteristics in AlGaN / GaN HEMT ' s," *Journal of Modern Physics, 2012, 3, 881-886*, vol. 2012, no. August, pp. 881–886, 2012.

[112] D. Streit, R. Lai, A. Oki, and A. Gutierrez-Aitken, "InP HEMT and HBT applications beyond 200 GHz," *Conference Proceedings. 14th Indium Phosphide and Related Materials Conference (Cat. No.02CH37307)*, 2002.

[113] J. G. Rathmell and A. E. Parker, "Circuit Implementation of a Theoretical Model of Trap Centres in GaAs and GaN Devices," vol. 6798, p. 67980R–67980R–11, Dec. 2007.

[114] N. I. C. H. Mclelland, M. C. Holland, M. R. S. Taylor, and S. P. Beaumont, "PSEUDOMORPHIC HEMT SMALL SIGNAL EQUIVALENT CIRCUIT MODEL SCALING," vol. 6, pp. 0–5, 1994.

[115] G. González, *Microwave Transistor Amplifiers : Analysis and Design*, Second Ed. John Wiley, 1997.

[116] L. Sang and J. E. Schutt-Aine, "AN IMPROVED NONLINEAR CURRENT MODEL FOR GAN HEMT HIGH POWER AMPLIFIER WITH LARGE GATE PERIPHERY," *Journal of Electromagnetic Waves and Applications*, vol. 26, no. 2–3, pp. 284–293, Jan. 2012.

[117] W. R. Curtice, "A MESFET Model for Use in the Design of GaAs Integrated Circuits," *IEEE Transactions on Microwave Theory and Techniques*, vol. 28, no. 5, pp. 448–456, May 1980.

[118] H. Statz, P. Newman, I. W. Smith, R. A. Pucel, and H. A. Haus, "GaAs FET device and circuit simulation in SPICE," *IEEE Transactions on Electron Devices*, vol. 34, no. 2, pp. 160–169, Feb. 1987.

[119] A. J. McCamant, G. D. McCormack, and D. H. Smith, "An improved GaAs MESFET model for SPICE," *IEEE Transactions on Microwave Theory and Techniques*, vol. 38, no. 6, pp. 822–824, Jun. 1990.

[120] D. A. J. Moran, K. Kalna, E. Boyd, F. McEwan, H. McLelland, L. L. Zhuang, C. R. Stanley, A. Asenov, and I. Thayne, "Self-aligned 0.12 µm T-gate In/sub .53/Ga/sub .47/As/In/sub .52/Al/sub .48/As HEMT technology utilising a non-annealed ohmic contact strategy," in *Electrical Performance of Electrical Packaging (IEEE Cat. No. 03TH8710)*, 2003, pp. 315–318.

[121] A. Bouloukou, B. Boudjelida, A. Sobih, S. Boulay, J. Sly, and M. Missous, "Design of low leakage InGaAs/InAlAs pHEMTs for wide band (300MHz to 2GHz) LNAs," in *ASDAM 2008 - Conference Proceedings of the 7th International Conference on Advanced Semiconductor Devices and Microsystems*, 2008, pp. 79–82.

[122] D. Schreurs, Y. Baeyens, K. Van der Zanden, J. Verspecht, M. Van Hove, W. De Raedt, B. Nauwelaers, and M. Van Rossum, "Large-signal HEMT modelling, specifically optimized for InP based HEMTs," in *Proceedings of 8th International Conference on Indium Phosphide and Related Materials*, 1996, pp. 638–641.

[123] H. Fukui, "Determination of the Basic Device Parameters of a GaAs MESFE," *Bell System Technical Journal*, vol. vol. 58, pp. 771–797, 1979.

[124] A. Sobih, "MMIC Broadband Low Noise Amplifiers for the Square Kilometre Array Radio Telescope," The University of Manchester, Manchester, 2007.

[125] B. Boudjelida, A. Sobih, S. Arshad, A. Bouloukou, S. Boulay, J. Sly, and M. Missous, "Sub-0.5 dB NF broadband low-noise amplifier using a novel InGaAs/InAlAs/InP pHEMT," in *ASDAM 2008 - Conference Proceedings of the 7th International Conference on Advanced Semiconductor Devices and Microsystems*, 2008, pp. 75–78.

[126] M. W. Pospieszalski and E. J. Wollack, "Ultra-low-noise, InP field effect transistor radio astronomy receivers: state-of-the-art," in *13th International Conference on*

Microwaves, Radar and Wireless Communications. MIKON - 2000. Conference Proceedings (IEEE Cat. No.00EX428), 2000, vol. 3, pp. 23–32.

[127] I.J.Bahl, *Fundamentals of RF and Microwave Transistor Amplifiers*. John Wiley & Sons, Inc,2009.

[128] H. A. Haus and R. B. Adler, “Optimum Noise Performance of Linear Amplifiers,” *Proceedings of the IRE*, vol. 46, 1958.

[129] W. Haensch, E. J. Nowak, R. H. Dennard, P. M. Solomon, A. Bryant, O. H. Dokumaci, A. Kumar, X. Wang, J. B. Johnson, and M. V. Fischetti, “Silicon CMOS devices beyond scaling,” *Ibm Journal of Research and Development*, vol. 50, no. 4.5, pp. 339–361, Jan. 2006.

[130] R. Grundbacher, J. Uyeda, R. Lai, D. Umemoto, P. H. Liu, M. Barsky, A. Cavus, L. J. Lee, J. Chen, J. Gonzalez, S. Chen, T. Block, and A. Oki, “High performance millimeter wave 0.1 µm InP HEMT MMIC LNAs fabricated on 100 mm wafers,” in *16th IPRM. 2004 International Conference on Indium Phosphide and Related Materials, 2004.*, 2004, pp. 284–287.

[131] D.-H. Kim and J. a. del Alamo, “30-nm InAs Pseudomorphic HEMTs on an InP Substrate With a Current-Gain Cutoff Frequency of 628 GHz,” *IEEE Electron Device Letters*, vol. 29, no. 8, pp. 830–833, Aug. 2008.

[132] Y. Mimino, M. Hirata, K. Nakamura, K. Sakamoto, Y. Aoki, and S. Kuroda, “High gain-density K-band P-HEMT LNA MMIC for LMDS and satellite communication,” *2000 IEEE Radio Frequency Integrated Circuits (RFIC) Symposium Digest of Papers (Cat. No.00CH37096)*, pp. 209–212.

[133] “GaAs MMICs for wireless transceiver components - Electronic Products.” [Online]. Available: http://www2.electronicproducts.com/GaAs_MMICs_for_wireless_transceiver_components-article-MMIC-sep1994-html.aspx. [Accessed: 13-Aug-2013].

[134] L. Y. Chu, E. Fischer, S. W. Duncan, N. E. Byer, and S. Weinreb, “Wideband MMIC receiver modules for imaging array applications,” in *Aerospace/Defense Sensing and Controls*, 1998, pp. 46–56.

[135] M. Stiglitz and C. Blanchard, “MMIC Design: GaAs FETs and HEMTs.,” *Microwave Journal*, Oct. 1989.

[136] R. Ludwig and G. Bogdanov, *RF circuit design :theory and applications*. Pearson/Prentice Hall, 2009.

[137] Hong Shen et.al, “Fabrication and characterization of thin film resistors for GaAs-based power amplifiers,” *Int conf on comp semicond manuf tech, CS ManTech*, vol. Vol. 3., 2003.

[138] R. Sharma and S. Vinayak, “RF parameter extraction of MMIC nichrome resistors,” *Microwave and …*, 2003.

[139] “5 Coplanar Elements --- Coplanar Interdigital Capacitor C_IDC.” [Online]. Available: http://www.imst.de/coplan/online_manual/c_idc.html. [Accessed: 20-Feb-2013].

[140] K. W. Ian and M. Missous, “Thermally stable In 0.7 Ga 0.3 As/In 0.52 Al 0.48 As pHEMTs using thermally evaporated palladium gate metallization,” *Semiconductor Science and Technology*, vol. 29, no. 3, p. 035009, Mar. 2014.

[141] F. Packeer, M. Mohamad Isa, W. Mat Jubadi, K. W. Ian, and M. Missous, “Fabrication and characterization of tensile In 0.3 Al 0.7 As barrier and compressive In 0.7 Ga 0.3 As channel pHEMTs having extremely low gate leakage for low-noise applications,” *Journal of Physics D: Applied Physics*, vol. 46, no. 26, p. 264002, Jul. 2013.

[142] R. W. Jung-Suk Goo; Hee-Tae Ahn; Ladwig, D.J.; Zhiping Yu; Lee, T.H.; Dutton, “A noise optimization technique for integrated low-noise amplifiers,” *Solid-State Circuits, IEEE Journal of , vol.37, no.8, pp.994, 1002, Aug 2002*, vol. 37, no. 8, pp. 994–1002, Aug. 2002.

[143] A. B. Ibrahim, M. N. Hussain, A. R. Othman, and M. S. Johal, “Low Noise Amplifier at 5 . 8GHz with Cascode and Cascaded Techniques Using T-Matching Network for Wireless Applications,” vol. 1, no. 1, pp. 1–8, 2011.

[144] Y. Peng, K. Lu, and W. Sui, “A 7- TO 14-GHz GaAs pHEMT LNA WITH 1 . 1 dB NOISE FIGURE AND 26 dB GAIN,” vol. 52, no. 11, pp. 2615–2617, 2010.

[145] L. Liu, A. R. A. S. Member, H. Benedickter, and C. R. B. Fellow, “InP / GaInAs pHEMT Ultralow-Power Consumption MMICs,” pp. 3–6, 2011.

[146] W. Xiao-mei, S. Zheng-wen, C. Yong, and W. Si-xiu, “Design and Analysis of an X-band Low Noise Amplifier,” *2010 Second International Conference on Multimedia and Information Technology*, pp. 278–282, 2010.

[147] R.Tsu and L.Esaki, “Tunnel Diodes (Esaki Diode) Part I Tunnel Diode principles Concept of Electron Tunneling,” 1973.

[148] T. H. E. Faculty and O. F. Engineering, “ADVANCED InGaAs-AlAs RTD FOR ULTRA HIGH SPEED DIGITAL,” pp. 1–56, 2013.

[149] D. Dragoman and M. Dragoman, “Terahertz fields and applications,” *Progress in Quantum Electronics*, vol. 28. 2004.

[150] J. N. Schulman, H. J. De Los Santos, and D. H. Chow, “Physics-based RTD current-voltage equation,” *IEEE Electron Device Letters*, vol. 17, no. 5, pp. 220–222, May 1996.

[151] G. I. H. P. M. J. N. S. Jian Ping Sun, “Resonant tunneling diodes: Models and properties.”

[152] M. A. Zawawi, K. W. Ian, J. Sexton, and M. Missous, “Fabrication of Submicrometer InGaAs/AlAs Resonant Tunneling Diode Using a Trilayer Soft Reflow Technique With Excellent Scalability,” *IEEE Transactions on Electron Devices*, vol. 61, no. 7, pp. 2338–2342, Jul. 2014.

[153] E.F. Schubert, “Resonant-tunneling-structures.” [Online]. Available: http://www.ecse.rpi.edu/~schubert/Course-ECSE-6290-SDM-Resonant-tunneling-structures.pdf.

[154] Emanuela Buccafurri, “Analytical Modeling of Silicon Based Resonant Tunneling Diode for RF Oscillator Application,” Lyon University, 2010.

[155] J. P. Sun, G. I. Haddad, L. Fellow, P. Mazumder, S. Member, and J. N. Schulman, “Resonant Tunneling Diodes : Models and Properties,” *Proc. of the IEEE, Vol. 86, No. 4, April 1998*, vol. 86, no. 4, 1998.

[156] Mohamad Adzhar Bin Md Zawawi, “Advanced In0.8Ga0.2As/AlAs Resonant Tunneling Diodes for Applications in Integrated mm-waves MMIC Oscillators,” The University of Manchester, 2015.

[157] I. Abramov and I. Goncharenko, “Simulation of GaAs/AlGaAs RTD using One-Band Combined Model,” in *2006 16th International Crimean Microwave and Telecommunication Technology*, 2006, vol. 2, pp. 665–666.

[158] A. Sigurdardottir, V. Krozer, and H. L. Hartnagel, “Modeling and design of InAs/AlSb-resonant tunneling diodes,” *Applied Physics Letters*, vol. 67, no. 22, p. 3313, 1995.

[159] T. S. Moise, Y.-C. Kao, a. J. Katz, T. P. E. Broekaert, and F. G. Celii, “Experimental sensitivity analysis of pseudomorphic InGaAs/AlAs resonant-tunneling diodes,” *Journal of Applied Physics*, vol. 78, no. 10, p. 6305, 1995.

[160] A. Shahhoseini, S. Ghorbanalipour, and R. Faez, “Detemining the Thickness of Barriers and Well of Resonance Tunneling Diodes by Specified I-V Characteristic,” *Applied Mechanics and Materials*, vol. 110–116, pp. 5464–5470, Oct. 2011.

[161] M. Baudrit and C. Algora, “Tunnel diode modeling, including nonlocal trap-assisted tunneling: A focus on IIIV multijunction solar cell simulation,” *IEEE Transactions on Electron Devices*, vol. 57, pp. 2564–2571, 2010.

[162] ATLAS Silvaco, “The Simulation Standard, Simulation of Resonant Tunneling Diodes Using ATLAS.”

[163] Cheng.P, “Novel Tunneling Barrier Designs for Resonant Tunneling diodes,” Stanford University, 1991.