TECHNIQUE OF FAILURE ANALYSIS FOR GATE OXIDE DEFECT OF BI-POLAR CMOS DIFFUSE (BCD) TECHNOLOGY

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ABSTRACT

This research presents failure analysis (FA) works on gate oxide defect of Bi-polar CMOS Diffuse (BCD) technology. The latent problem with electrical degradation in the CMOS performance is due to gate oxide defect. The defect was well known affects the CMOS reliability after certain period of time, temperatures and stress. The FA techniques used for this research were developed using a combination of I_{DDQ} scan test pattern, photo localization by the emission microscope and Field Emission Scanning Electron Microscopy (FE-SEM) for defect inspection. The FA methods successfully evaluated on few failing samples which were taken from customer return with I_{DDQ} failure range from 50µA until less than 1mA. Concurrently, the spotted excessive emission found on the defective samples during photo localization step indicates of gate oxide defect. The defect well observed with FE-SEM analysis on all tested samples after the physical analysis accomplishment until oxide layer. The proposed technique shows an effective method to compensate the existing FA difficulty on gate oxide defect faced by IC manufacturer in micrometer and nanometer scale technology, which having more metal interconnection layers with higher dense. The proposed technique able to construct promising result compared to the conventional techniques which used in the current FA practice due to certain extends of limitation.

ABSTRAK

Penyelidikan ini menerangkan mengenai analisis kegagalan pada lapisan pintu oksida bagi teknologi Bipolar CMOS Diffuse (BCD). Teknik analisis kegagalan ini menggunakan gabungan ujian data imbasan arus dalam keadaan statik (I_{DDQ}), disamping penggunaan mikroskop foto pemancaran dan Field Emission Scanning Electron Microscopy (FE-SEM) untuk pemeriksaan kegagalan. Analisis kegagalan dilakukan dengan menggunakan sampel yang diambil daripada aplikasi pelanggan yang telah rosak dengan julat kegagalan I_{DDQ} diantara 50µA sehingga kurang daripada 1mA. Semasa analysis kegagalan dilakukan dengan menggunakan kaedah foto pemancar, lebihan cahaya yang dijumpai pada litar bersepadu yang rosak menunjukkan simptom awal yang disebabkan oleh kegagalan pada pintu pagar oksida. Kegagalan ini dapat dibuktikan semasa proses fizikal terhadap sampel dan kemudian pemeriksaan dengan menggunakan FE-SEM. Teknik analisis kegagalan ini mencadangkan satu kaedah yang lebih efektif bagi menyelesaikan permasalahan yang dihadapi oleh pengeluar IC untuk melakukan ujian kegagalan lapisan pintu oksida dalam teknologi berskala mikro dan nano. Kesimpulannya, teknik ini didapati mampu menghasilkan keputusan yang lebih baik berbanding dengan teknik-teknik lazim yang digunakan sebelum ini. Ini disebabkan oleh beberapa faktor yang dikenalpasti telah menghadkan penggunaannya di dalam teknologi analisis kegagalan.

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LIST OF ABBREVIATIONS

AFP	-	Atomic Force Probe
APG	-	Automotive Product Group
ATE	-	Automatic Test Equipment
ATPG	-	Automated Test Program Generation
BCD	-	Bipolar CMOS DMOS
BGA	-	Ball Grid Array
BICS	-	Built In Current Sensor
CCD	-	Charge Couple Device
CMOS	-	Complementary Metal Oxide Semiconductor
CPU	-	Central Processing Unit
DfT	-	Design for Testability
DUT	-	Device under Test
EOS	-	Electrical Over Stress
ESD	-	Electro Static Discharge
EMI	-	Electro Magnetic Interference
EWS	-	Electrical Wafer Sort
FA	-	Failure Analysis
FE-SEM	-	Field Emission Scanning Electron Microscopy
FT	-	Final Test
GND	-	Ground
GOX	-	Gate Oxide
HSPICE	-	High Simulation Program with Integrated Circuit Emphasis
HVM	-	High Volume Manufacturing
IC	-	Integrated Circuit
I/O	-	Input Output

I/V	-	Current/Voltage
I_{DDQ}	-	Supply current in the quiescent state
IMD	-	Intermediate Metal Dielectric
I.V	-	Current Voltage measurement
LVS	-	Layout versus Schematic
MiNT-SRC	-	Microelectronics and Nanotechnology-Shamsuddin Research Centre
MOSFET	-	Metal Oxide Semiconductor Field Effect Transistor
NIR	-	Near Infra Red
OrCAD	-	Software tools for electronic design automation
PIQ	-	Polymide Isoindro Quirazorindione
PMD	-	Pre-Metal Dielectric
PMU	-	Precision Measurement Unit
PTS	-	Power Train and Safety
Q.E	-	Quantum Efficiency
SA0	-	Stuck At '0'
SA1	-	Stuck At '1'
SEM	-	Scanning Electron Microscopy
SPI	-	Serial Peripheral Interface
SDI	-	Serial Data In
SDO	-	Serial Data Out
TPG	-	Test Program Generation
UTHM	-	Universiti Tun Hussein Onn Malaysia
VLSI	-	Very Large Scale Integration
P-MOS	-	P channel MOS
N-MOS	-	N channel MOS
V_{DD}	-	Voltage Supply
V_{SS}	-	GND path

LIST OF PUBLICATION

1. Farisal Abdullah, Nafarizal Nayan, Muhammad Mahadi Abdul Jamil, and Norfauzi Kamsin : “IDD scan test method for fault localization technique on CMOS VLSI failure analysis”, ICSE Proc. 2010, Melaka.

2. Farisal Abdullah, Nafarizal Nayan, and Muhammad Mahadi Abdul Jamil : “Failure analysis using IDD current leakage and photo localization for gate oxide defect of CMOS VLSI”, SCORED 2010, Putrajaya.

CHAPTER 1

INTRODUCTION

1.1 Research background

Since the last two decades, electronic industry has growth rapidly. Demand from the numerous segments of industries such as computing, automotive, telecommunication, and industrial product, results the microelectronics evolution become more complex.

The integrated circuit (IC) voltage supply (V_{DD}) reduces gradually following by the demand of speed, lower power consumption and reliability concern [1]. Hence, decreasing the transistor threshold voltage (V_{th}) essentially not only ensures higher drive current but also improves the IC speeds. This factor makes the macro-model works on leakage power studies become more challenge [2]. D. Frank *et al*., (2001) clarify the challenge in the future scaling down of the CMOS supply voltage which proportional with the electronics application. Present of lower V_{th} value was found not only reduce the supply current in the quiescent state (I_{DDQ}), but also amplify the leakage power indeed.

Impact from this evolution, I_{DDQ} current may found undersized and become more complex to discriminate between the good and fail IC. Thus, screen method at the production test also needs to be revising [3]. On the other hand, failure analysis (FA) method needs more creativity to compensate the trend as well [4-8]. As a progress, David P. Vallet (2002) has presented the FA requirement on the

nanoelectronics IC technology, which elaborates this concern. The FA challenges and techniques may penetrate a new chapter of IC diagnostic evolution [9]-[10].

Hurst S, (1998) and Bushnell M and Agrawal V, (2000) emphasize the scan test that become vital elements on the modern digital and mixed-signal VLSI circuit testing [11]-[13]. Rochit Rajsuman, (2000) further elaborate by incorporate the I_{DDQ} test into the scan test algorithm contribute significant yield improvement on the integrated circuit quality [14]. Thus these test combination makes the overall scan test become efficient to resolve the digital circuit performance especially to monitor the earlier gate oxide (GOX) failure.

The increasing number of GOX failure due to wear out phase has motivate further researcher to improve the existing wafer process and explorer new process method. The typical factors that brought out the IC become fail are during stress condition in the application environment. Therefore, there is strong requirement to develop a new approach on the specific FA technique to detect GOX defect on BCD integrated circuit. The improvement is to recommend an alternative solution for the scan failure which typically occurs on the digital logic circuit, by using proposed method cited from Design for Testability (DfT) methodology.

1.2 Problems statement

In failure analysis terminology, probe technique becomes one of the well-known methods to perform signal analysis on the BCD technology device [15]. This technique has an ability to perform signal acquisition from the probe pad, restricted logic block until to the single transistor cell. However, due to limitation on it sizes and cost, evolution on the modern FA method has progressively challenged this technique.

In existing market, the most fashionable probes are active probe and passive probe which available in several size, micro, nano and pico. The selection on it size is relying on the tested circuit been done. For single transistor cell measurement, the most accurate tool been use in nowadays FA technique is Atomic Force Probe (AFP). This technique is viable to perform comprehensive current-voltage (I-V) characteristic of the single cell which consists of Drain, Gate, Source and Well. However in term of cost-effective method AFP was consider costly compared with probe technique.

Figure 1.1 shows reduction of the gate length in BCD technology and escalating of metal interconnection levels in parallel. This combination has challenge the gate oxide reliability since the device will perform faster during switching operation. Therefore, restriction on the gate oxide failure makes the probe method become ineffective to localize the defect during FA. Modern lithography process on the BCD device is dramatically shirked from millimetre, down to below 90nm scale. This factor contributes complication on the FA method during perform a signal analysis on the micro block circuit which consist of latches and combinational logic.

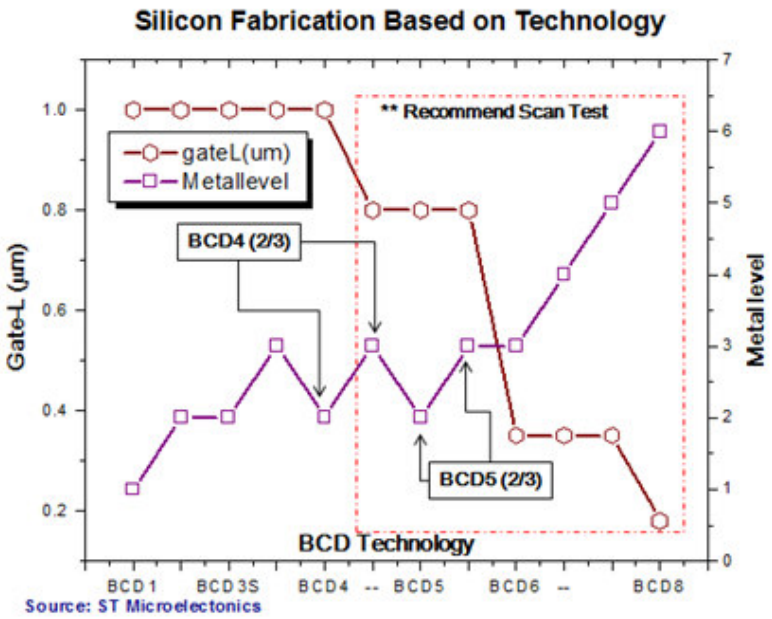

Figure 1.1: The reduction of gate length in lithography technology and escalating of metal level influence the probing techniques due to scale constraint [16].

This research recommends using the I_{DDQ} scan test which typically used for the IC testing as a FA method. I_{DDQ} scan test is incorporate from the Automatic Test Pattern Generation (ATPG) method which able to stimulated limited of test vectors with higher fault coverage. This scan test is particularly to exercising the P-MOS and N-MOS transistor switching on the latches and combination logics, whereby any leaky transistor junction can be identify during the fault localization.

Failure analysis is a combination of few steps of procedure to define the possible root cause which occurs on the defective IC. The FA method may consist of combination between the testing information and appropriate diagnosis step to identify the physical defect on the IC based on the failure mode [17]. The FA method could be varies, depend on how complex the device was failed and challenge to replicate the failure mode for FA purpose.

In most events, FA becomes crucial constructive steps to translate the failure mode into an isolated area. Hereby it becomes an evolution process from the past experienced data, present use and future challenge [18].

1.2.1 Background of current FA on BCD technology.

During FA, to perform fine signal characterization on the restrict logic cell; failure analyst has to perform extra probing method on the test point besides using the external leads for voltage supply and others input/output (I/O) pins.

Typically, the test points are visible on the silicon, and they are locating at the same level as the bond pad area. The visible points are not covering by the protection layer to make it easy to contact with. The main purpose to have these test points is after the wafer fabrication process is completed, every single die inside the wafer has to undergo parametric test to validate whether it has been fabricated with correct recipe according to spec or not. This test screen at the wafer side is known as an electrical wafer sort (EWS). In this case, the numbers of test points are limited and only covering the overall parameters of the die, and not to extend until the logic cell functionality. Therefore, it is essential to have more electrical information in order to drive the defect localization during the FA works [19].

In order to overcome this challenge, failure analyst has to access underneath interconnection in order to obtain the desired signal. This signal measurement can be used by the combination between laser-cut tool and active or passive probe tip. The advantage of using probing technique is, it has to provides electrical contact directly to the restrict logic block. Commonly the desired interconnection layer are present at underneath layer where all the transistors been connected together after it been fabricated deeply in the active area [20]. Takeshi Nokuo *et al.,* (2007) and S.L Toh *et al*., (2007), propose a conducive FA method using probing technique on nanometre device to demonstrate the probing competency.

Nevertheless, the main constraint is that not all the test points are utilize for IC diagnose in particular for scan type of failure. Even though the unforeseen underneath interconnection net is possible to reach by using probing method, uncomplimentary it may create signal distortion or interference from untested digital block inside the same IC. In few specific types of failing IC which related to the digital CMOS circuit, this method found impractical to utilize for failure analysis at all. Figure 1.2 shows the illustration of few critical points on the interconnection, concise of gap, width, and level, whereas compulsory for the probing method to obtain the signals during the failure analysis works.

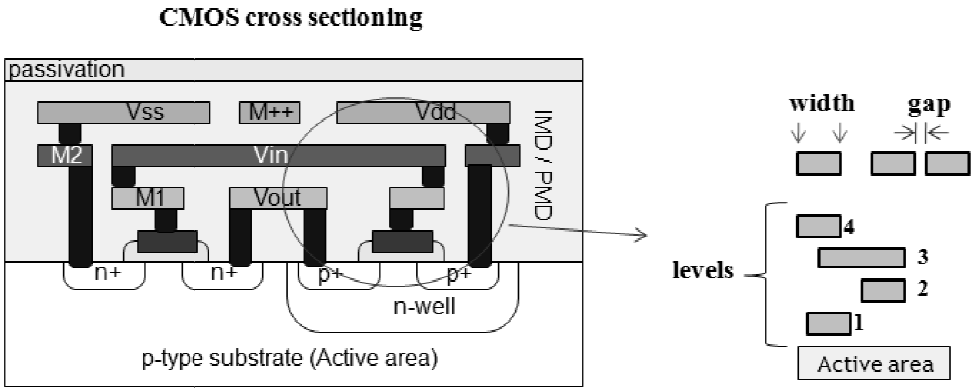

Figure 1.2: The lithography process describe the metal lines width, gap between them and space between metal layers [15].

1.2.2 Probing Method Challenge for Currently BCD FA.

For FA step using probing method, few constrain factors were identified as the metal interconnection increase on the BCD technology. In other words, this method has a tendency to cause damaged on the silicon and only limit to a few numbers of signal measurement per one time, i.e. I-V characteristic. During this step, there is a critical path that may induce damaged on the IC surface. The step begins when the probe tip starts moving from the zero position towards the desired probing points, either on the silicon or at particular underneath the metal line (after considered the top protection layer been removed using the laser-cut method).

In worst case simulation, if the probe tip has found unintentionally vibrate or wrongly positioning on the target point due to mishandling (by human factor) or vibration on probing station (by equipment stability factor), it may result of massive interconnection damaged. Figure 1.3 shows an evident in the interconnection damage result from the worst-case simulation due to mishandling event.

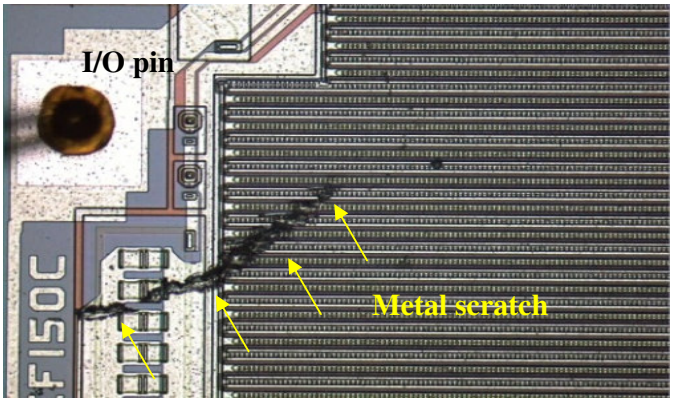

Figure 1.3: The example of damage on the silicon due to probing method [21].

As a consequence, the IC becomes malfunction by default and no longer can operate as the pre-probing step. The internal circuit of the IC probably can be either 'open' or 'short' circuit. This unforeseen circumstance becomes a fear to the analyst or FA engineer since commonly the numbers of failing sample for this specific failure mode are limited.

Another point in probing method is it only can acquire a limited number of signal measurements due to constraint between the probes versus probe point. Figure 1.4 shows the limitation on the nano-probe competency during the signal measurement on the restrict circuit. The signal measurement using limited numbers of nano-probes were only works on the desired transistor or logic circuit. Thus it is not well proficient to use in larger digital logic block [15,20].

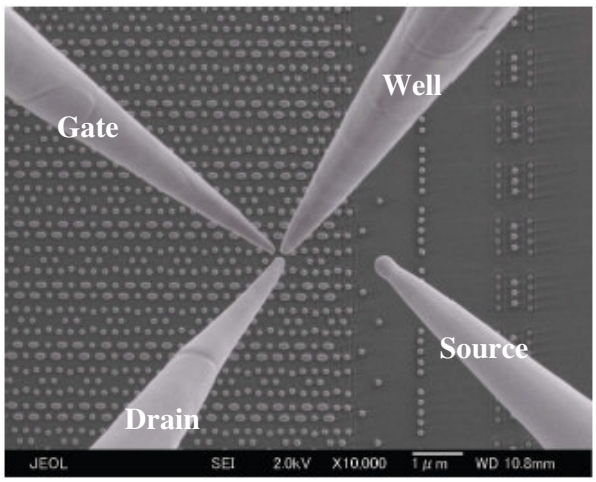

Figure 1.4: A SEM image showing four nano-probes at the source, drain, gate and well contacts of a transistor cell [20].

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