

TECHNIQUE OF FAILURE ANALYSIS FOR GATE OXIDE DEFECT OF
BI-POLAR CMOS DIFFUSE (BCD) TECHNOLOGY

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In the name of Allah, The Most Gracious and The Most Merciful.

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ABSTRACT

This research presents failure analysis (FA) works on gate oxide defect of Bipolar CMOS Diffuse (BCD) technology. The latent problem with electrical degradation in the CMOS performance is due to gate oxide defect. The defect was well known affects the CMOS reliability after certain period of time, temperatures and stress. The FA techniques used for this research were developed using a combination of I_{DDQ} scan test pattern, photo localization by the emission microscope and Field Emission Scanning Electron Microscopy (FE-SEM) for defect inspection. The FA methods successfully evaluated on few failing samples which were taken from customer return with I_{DDQ} failure range from $50\mu A$ until less than $1mA$. Concurrently, the spotted excessive emission found on the defective samples during photo localization step indicates of gate oxide defect. The defect well observed with FE-SEM analysis on all tested samples after the physical analysis accomplishment until oxide layer. The proposed technique shows an effective method to compensate the existing FA difficulty on gate oxide defect faced by IC manufacturer in micrometer and nanometer scale technology, which having more metal interconnection layers with higher dense. The proposed technique able to construct promising result compared to the conventional techniques which used in the current FA practice due to certain extends of limitation.

ABSTRAK

Penyelidikan ini menerangkan mengenai analisis kegagalan pada lapisan pintu oksida bagi teknologi Bipolar CMOS Diffuse (BCD). Teknik analisis kegagalan ini menggunakan gabungan ujian data imbasan arus dalam keadaan statik (I_{DDQ}), disamping penggunaan mikroskop foto pemancaran dan Field Emission Scanning Electron Microscopy (FE-SEM) untuk pemeriksaan kegagalan. Analisis kegagalan dilakukan dengan menggunakan sampel yang diambil daripada aplikasi pelanggan yang telah rosak dengan julat kegagalan I_{DDQ} diantara $50\mu\text{A}$ sehingga kurang daripada 1mA . Semasa analisis kegagalan dilakukan dengan menggunakan kaedah foto pemancar, lebih cahaya yang dijumpai pada litar bersepadu yang rosak menunjukkan simptom awal yang disebabkan oleh kegagalan pada pintu pagar oksida. Kegagalan ini dapat dibuktikan semasa proses fizikal terhadap sampel dan kemudian pemeriksaan dengan menggunakan FE-SEM. Teknik analisis kegagalan ini mencadangkan satu kaedah yang lebih efektif bagi menyelesaikan permasalahan yang dihadapi oleh pengeluar IC untuk melakukan ujian kegagalan lapisan pintu oksida dalam teknologi berskala mikro dan nano. Kesimpulannya, teknik ini didapati mampu menghasilkan keputusan yang lebih baik berbanding dengan teknik-teknik lazim yang digunakan sebelum ini. Ini disebabkan oleh beberapa faktor yang dikenalpasti telah menghadkan penggunaannya di dalam teknologi analisis kegagalan.

TABLE OF CONTENT

TITLE	i
DECLARATION	ii
ACKNOWLEDGEMENTS	iii
ABSTRACT	iv
ABSTRAK	v
CONTENT	vi
LIST OF TABLES	x
LIST OF FIGURES	xi
LIST OF ABBREVIATIONS	xvi
LIST OF PUBLICATIONS	xviii
CHAPTER 1	
INTRODUCTION	1
1.1 Research background	1
1.2 Problem statement	3
1.2.1 Background of current FA on BCD technology	5
1.2.2 Probing Method Challenge for Currently BCD FA	6
1.2.3 Scan test opportunity for FA on CMOS VLSI	8
1.3 Objective of study	10
1.4 Scope of work	11
1.5 Thesis outline	12

CHAPTER 2	LITERATURE REVIEW	13
2.1	Definition of CMOS VLSI Failure Analysis	14
2.2	Digital logic circuit and testing	15
2.2.1	ASIC device on the VLSI circuit	15
2.2.2	Digital logic test for CMOS VLSI	17
2.3	Digital circuit fault modeling	20
2.3.1	Logical fault model	21
2.3.2	I_{DDQ} fault model	26
2.4	Fault coverage	29
2.5	The Structure of Gate Oxide (GOX)	31
2.5.1	Micro structure and bond energy of SiO_2	32
2.5.2	Reliability of Gate Oxide in wafer	33
2.5.3	Breakdown of Gate Oxide	35
2.5.4	Gate Oxide's leakage current	37
2.6	Fault Localization Analysis	39
2.6.1	Photo Emission Microscope Principle	40
2.6.2	Field Emission Scanning Electron Microscopy (FESEM)	47
2.7	Previous FA work on CMOS VLSI	49
2.8	Summary	52
CHAPTER 3	METHODOLOGY	53
3.1	Fault localization using PEM	56
3.2	ATPF Scan Test	57
3.2.1	I_{DDQ} scan test pattern algorithm	58
3.2.2	Measurement result of I_{DDQ} current timing	62

3.3	Sample Preparation	64
3.3.1	Front side of sample preparation	66
3.2.2	Backside of sample preparation	71
3.2.3	Sample preparation for experiment	80
3.4	Physical analysis and defect identification	81
3.4.1	Silicon die de-processing analysis	81
3.4.2	FE-SEM for topography observation	82
3.5	Summary	83

CHAPTER 4 RESULT AND DISCUSSION 84

4.1	I_{DDQ} software simulation with GOX defect oriented	87
4.1.1	Ohmic soft defect on the CMOS inverter	87
4.1.2	Ohmic soft defect on OR logic circuit	89
4.2	I_{DDQ} current measurement result	93
4.2.1	Ohmic hard defect on the logic circuit	95
4.2.2	Leakage estimation on the benchmark circuit	96
4.2.3	Leakage timing and measurement on the tested circuit	97
4.2.4	Scan test pattern on the tested circuit	102
4.3	Photo emission and die level topography analysis	107
4.4	Emission Result and Failure Mechanism	112
4.5	Summary	114

CHAPTER 5	CONCLUSION AND RECOMMENDATION	115
5.1	Conclusion	115
5.2	Recommendation and Future Work	117
	REFERENCES	119
	APPENDIX A	128
	APPENDIX B	130
	APPENDIX C	132



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LIST OF TABLES

Table 2.1	Integration levels on the digital circuit	15
Table 2.2	Fundamental of logic gates structures	17
Table 2.3	Input patterns complexity for combinational logic output	20
Table 2.4	Type of fault localization techniques for CMOS VLSI FA	39
Table 2.5	FA outcome from previous work consist of tools and methods	50
Table 3.1	CMOS VLSI IC features trend on BCD technology	53
Table 3.2	The microscope objective lens limitation between two methods of sample preparation	78
Table 3.3	Sample preparation summary for the defective IC	80
Table 4.1	The table shows how the matrix fault works based on the test vector	86
Table 4.2	Individual MOS conditions correspond to input logic, V_{IN} biasing to pull-down the current supply, I_{DDQ} to GND	89
Table 4.3	Elevate I_{DDQ} current during the scan test on the fault free transistor cell	91
Table 4.4	Elevate I_{DDQ} current during the scan test on the faulty transistor cell	91
Table 4.5	Leakage estimation result for benchmark circuit	96
Table 4.6	I_{DDQ} current measurement result at different post-test time	99
Table 4.7	I_{DDQ} current measurement result at different post-test time with V-bump stress	100
Table 4.8	Elevate I_{DDQ} current result from the defective sample ICs	101

LIST OF FIGURES

Figure 1.1	The reduction of gate length in lithography technology and escalating of metal level influence the probing techniques due to scale constraint.	4
Figure 1.2	The lithography technologies influence the metal lines width, gap between them and space between metal layers.	6
Figure 1.3	The example of damage on the die surface due to probing method	7
Figure 1.4	A SEM image showing four nano-probes at the source, drain, gate and well contacts of a transistor.	7
Figure 1.5	Principle of open failure site detection with limited probe tip.	8
Figure 2.1	The digital ICs availability	16
Figure 2.2	Digital IC test set-up	17
Figure 2.3	Combinational logic input and output simplified block	19
Figure 2.4	The SAF model and its Boolean expression between fault free and faulty.	22
Figure 2.5	Circuit schematic represent the bridge fault events	24
Figure 2.6	(a) Illustration of inverter circuit proposed with gate to drain defect (b) I_{DDQ} signature subsequent due to the leakage	28 28
Figure 2.7	The effectiveness of I_{DDQ} scan test data from HP and IBM.	29
Figure 2.8	Cross section of NMOS	31
Figure 2.9	SiO_2 molecules bond geometry orientation	32
Figure 2.10	Bathtub Curve for Failures	33
Figure 2.11	3D CMOS Inverter structure with the expected current leakage	35
Figure 2.12	(a) Formation of Traps in the Gate-Oxide (b) Creation of Conduction Path through Traps in the Gate-Oxide (c) Increased Traps in Gate Oxide after Conduction (d) Cross Section of the Oxide after Hard Breakdown	36 36 36 36

Figure 2.13	Supply voltage trend with the threshold voltage scaling impact from the scaled CMOS technology nodes.	37
Figure 2.14	The hypothetical of all possible defect models present inside a CMOS inverter with equivalent schematic connections	38
Figure 2.15	Indirect radiative transitions involving (a) Phonons (b) impurities and hot carriers	41
Figure 2.16	Fundamental spectra of most well-known emissions	42
Figure 2.17	Spectral response of commercially available image intensifiers	43
Figure 2.18	(a) Hamamatsu Photonic PEM machine (b) The microscope station of the PEM machine	44 44
Figure 2.19	Broad light spectrum wavelength	45
Figure 2.20	(a) The camera sensitivity on the fault localizations tools (b) The emission result based on camera sensitivity	46 46
Figure 2.21	FESEM schematic	48
Figure 2.22	Current sensitivity versus lateral resolution of fault localization tools	51
Figure 3.1	Overall flow for the fault localization using I_{DDQ} scan test	55
Figure 3.2	(a) and (b): The comparison between proposed technique using scan test and old technique using probe	56
Figure 3.3	(a) and (b): The conceptual of scan test approach on the digital logic circuit.	58
Figure 3.4	The scan test flow on the digital logic circuit	60
Figure 3.5	Datalog results from the scan pattern test	60
Figure 3.6	Flowchart of test algorithm to senses the I_{DDQ} during the test pattern running.	61
Figure 3.7	I_{DDQ} measurement timing concept the ATE tester	62
Figure 3.8	The BCD technology die surface view and the circuit block allocation	65
Figure 3.9	Sample preparation equipments and steps	65
Figure 3.10	Expected upshot for the both sample preparation techniques	66
Figure 3.11	(a) The fine top metal line was found missing (peel-off) after the decapsulation step (b) The fine top metal line was found missing (peel-off) after the decapsulation step	67 67

Figure 3.12	(a) The conventional decapsulation procedure for type of plastic mold IC package	68
	(b) The enhance decapsulation procedure for BCD 5 and above IC technology	68
Figure 3.13	(a) to (e) Front side of sample preparation steps	69
Figure 3.14	Digital logic view from front side analysis using 5X objective lens	70
Figure 3.15	(a) The IC package subjected for cross sectioning and examines with FE-SEM	71
	(b) The cross section view of the IC package and the thickness measurement using FE-SEM	72
Figure 3.16	The opening on slug area with 3mm milling bit and the grinding consume computation	73
Figure 3.17	The thinning process of removing slug and pre-from layers	74
Figure 3.18	The remaining thickness layer after the thinning and polishing process has completed	75
Figure 3.19	(a) to (d): Sample preparation step by steps result	75
Figure 3.20	(a) Digital logic with 5X objective lens view from back side analysis using CCD camera.	76
	(b) Magnification of the digital logic with 20X objective lens from back side analysis using CCD camera.	76
Figure 3.21	(a) Digital logic view using 1X objective lens from back side analysis using IR camera.	77
	(b) Magnification of the digital logic view with 20x objective lens from back side analysis using IR camera.	77
Figure 3.22	Reflection loss in air-silicon interface by the incident light	79
Figure 3.23	Incident light reflection and absorption by the silicon substrate during imaging	79
Figure 4.1	The digital circuits block	86
Figure 4.2	The simulation result shows the test time improvement on the test mode condition compares to the normal mode	87
Figure 4.3	Ohmic defects model present of Inverter circuit	88
Figure 4.4	The ohmic short model affected by the p-Ch. M1 cell by using OrCAD simulations for I_{DDQ} current examines	90
Figure 4.5	Comparable elevated I_{DDQ} between faulty and fault free circuit	92

Figure 4.6	Measurement of elevated current from V_{DD} pin between the defect free and the defective IC	94
Figure 4.7	Measurement of elevated current on the 90nm CMOS technology using H-SPICE simulation	94
Figure 4.8	(a to d) Series of I-V characteristic on the defective IC versus good IC	95
Figure 4.9	Measurement on the I_{DDQ} value for the known good IC using the Teradyne A565 tester	97
Figure 4.10	I_{DDQ} current measurement during different test temperature	98
Figure 4.11	Software interface of the pattern generator using LabVIEW	102
Figure 4.12	Sample A: Over current failure on the defective IC	103
Figure 4.13	(a) Sample B: Scan test pattern sensitizes the failure on the diagnostic (HDG2) logic monitoring circuit	105
	(b) Sample B: Scan test pattern sensitizes the failure on the diagnostic (HDG2) logic monitoring circuit	105
Figure 4.14	(a) Good IC: Scan test pattern sensitizes the failure on the digital logic circuit controlled the voltage regulator (VSO1)	106
	(b) Sample C: Scan test pattern sensitizes the failure on the digital logic circuit controlled the voltage regulator (VSO1)	106
Figure 4.15	(a) Sample D; Under Normal Mode, the VCC and VCCM behavior found within the spec, same as good unit	107
	(b) Sample D; Under Test Mode, the VCC and VCCM behavior found within the spec, same as good unit	107
Figure 4.16	Sample A: FA result on 800nm CMOS using PEM method and defect identification using FE-SEM analysis during the chemically die delayering	108
Figure 4.17	Sample B: FA result on 1 μ m CMOS using PEM method and defect identification using FE-EM analysis during the chemically die delayering	109
Figure 4.18	Sample C: FA result on 600nm CMOS using PEM method and defect identification using FE-SEM analysis during the chemically die delayering	110
Figure 4.19	Sample D: FA result on 350nm CMOS using PEM method and defect identification using FE-SEM analysis during the parallel lapping step	111

Figure 4.20	The intensity profile obtained from the defective OR logic	112
Figure 4.21	Failure mechanism explained the physical defect	113



LIST OF ABBREVIATIONS

AFP	-	Atomic Force Probe
APG	-	Automotive Product Group
ATE	-	Automatic Test Equipment
ATPG	-	Automated Test Program Generation
BCD	-	Bipolar CMOS DMOS
BGA	-	Ball Grid Array
BICS	-	Built In Current Sensor
CCD	-	Charge Couple Device
CMOS	-	Complementary Metal Oxide Semiconductor
CPU	-	Central Processing Unit
DfT	-	Design for Testability
DUT	-	Device under Test
EOS	-	Electrical Over Stress
ESD	-	Electro Static Discharge
EMI	-	Electro Magnetic Interference
EWS	-	Electrical Wafer Sort
FA	-	Failure Analysis
FE-SEM	-	Field Emission Scanning Electron Microscopy
FT	-	Final Test
GND	-	Ground
GOX	-	Gate Oxide
HSPICE	-	High Simulation Program with Integrated Circuit Emphasis
HVM	-	High Volume Manufacturing
IC	-	Integrated Circuit
I/O	-	Input Output

I/V	-	Current/Voltage
I_{DDQ}	-	Supply current in the quiescent state
IMD	-	Intermediate Metal Dielectric
I.V	-	Current Voltage measurement
LVS	-	Layout versus Schematic
MiNT-SRC	-	Microelectronics and Nanotechnology-Shamsuddin Research Centre
MOSFET	-	Metal Oxide Semiconductor Field Effect Transistor
NIR	-	Near Infra Red
OrCAD	-	Software tools for electronic design automation
PIQ	-	Polymide Isoindro Quirazorindione
PMD	-	Pre-Metal Dielectric
PMU	-	Precision Measurement Unit
PTS	-	Power Train and Safety
Q.E	-	Quantum Efficiency
SA0	-	Stuck At '0'
SA1	-	Stuck At '1'
SEM	-	Scanning Electron Microscopy
SPI	-	Serial Peripheral Interface
SDI	-	Serial Data In
SDO	-	Serial Data Out
TPG	-	Test Program Generation
UTHM	-	Universiti Tun Hussein Onn Malaysia
VLSI	-	Very Large Scale Integration
P-MOS	-	P channel MOS
N-MOS	-	N channel MOS
V_{DD}	-	Voltage Supply
V_{SS}	-	GND path

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1. Farisal Abdullah, Nafarizal Nayan, Muhammad Mahadi Abdul Jamil, and Norfauzi Kamsin : “IDD scan test method for fault localization technique on CMOS VLSI failure analysis”, ICSE Proc. 2010, Melaka.
2. Farisal Abdullah, Nafarizal Nayan, and Muhammad Mahadi Abdul Jamil : “Failure analysis using IDD current leakage and photo localization for gate oxide defect of CMOS VLSI”, SCORED 2010, Putrajaya.



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CHAPTER 1

INTRODUCTION

1.1 Research background

Since the last two decades, electronic industry has growth rapidly. Demand from the numerous segments of industries such as computing, automotive, telecommunication, and industrial product, results the microelectronics evolution become more complex.

The integrated circuit (IC) voltage supply (V_{DD}) reduces gradually following by the demand of speed, lower power consumption and reliability concern [1]. Hence, decreasing the transistor threshold voltage (V_{th}) essentially not only ensures higher drive current but also improves the IC speeds. This factor makes the macro-model works on leakage power studies become more challenge [2]. D. Frank *et al.*, (2001) clarify the challenge in the future scaling down of the CMOS supply voltage which proportional with the electronics application. Present of lower V_{th} value was found not only reduce the supply current in the quiescent state (I_{DDQ}), but also amplify the leakage power indeed.

Impact from this evolution, I_{DDQ} current may found undersized and become more complex to discriminate between the good and fail IC. Thus, screen method at the production test also needs to be revising [3]. On the other hand, failure analysis (FA) method needs more creativity to compensate the trend as well [4-8]. As a progress, David P. Vallet (2002) has presented the FA requirement on the

nanoelectronics IC technology, which elaborates this concern. The FA challenges and techniques may penetrate a new chapter of IC diagnostic evolution [9]-[10].

Hurst S, (1998) and Bushnell M and Agrawal V, (2000) emphasize the scan test that become vital elements on the modern digital and mixed-signal VLSI circuit testing [11]-[13]. Rochit Rajsuman, (2000) further elaborate by incorporate the I_{DDQ} test into the scan test algorithm contribute significant yield improvement on the integrated circuit quality [14]. Thus these test combination makes the overall scan test become efficient to resolve the digital circuit performance especially to monitor the earlier gate oxide (GOX) failure.

The increasing number of GOX failure due to wear out phase has motivate further researcher to improve the existing wafer process and explorer new process method. The typical factors that brought out the IC become fail are during stress condition in the application environment. Therefore, there is strong requirement to develop a new approach on the specific FA technique to detect GOX defect on BCD integrated circuit. The improvement is to recommend an alternative solution for the scan failure which typically occurs on the digital logic circuit, by using proposed method cited from Design for Testability (DfT) methodology.



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1.2 Problems statement

In failure analysis terminology, probe technique becomes one of the well-known methods to perform signal analysis on the BCD technology device [15]. This technique has an ability to perform signal acquisition from the probe pad, restricted logic block until to the single transistor cell. However, due to limitation on it sizes and cost, evolution on the modern FA method has progressively challenged this technique.

In existing market, the most fashionable probes are active probe and passive probe which available in several size, micro, nano and pico. The selection on it size is relying on the tested circuit been done. For single transistor cell measurement, the most accurate tool been use in nowadays FA technique is Atomic Force Probe (AFP). This technique is viable to perform comprehensive current-voltage (I-V) characteristic of the single cell which consists of Drain, Gate, Source and Well. However in term of cost-effective method AFP was consider costly compared with probe technique.

Figure 1.1 shows reduction of the gate length in BCD technology and escalating of metal interconnection levels in parallel. This combination has challenge the gate oxide reliability since the device will perform faster during switching operation. Therefore, restriction on the gate oxide failure makes the probe method become ineffective to localize the defect during FA. Modern lithography process on the BCD device is dramatically shirked from millimetre, down to below 90nm scale. This factor contributes complication on the FA method during perform a signal analysis on the micro block circuit which consist of latches and combinational logic.

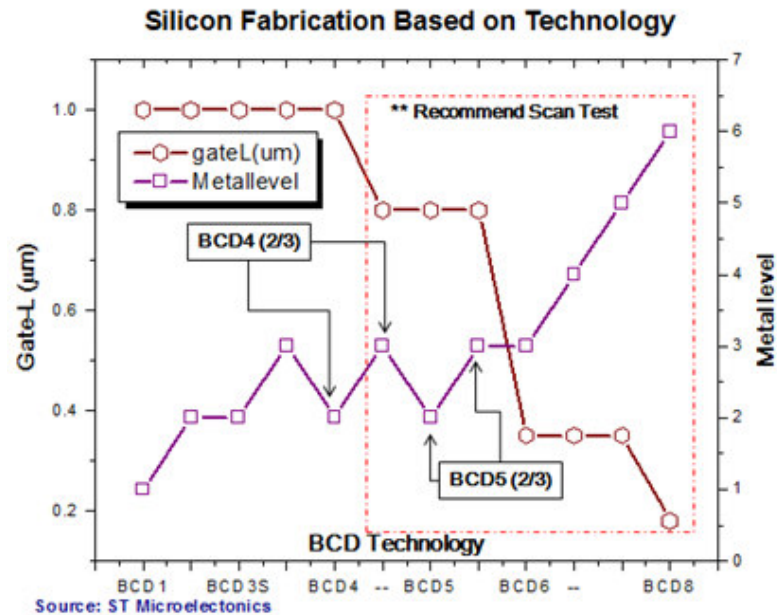


Figure 1.1: The reduction of gate length in lithography technology and escalating of metal level influence the probing techniques due to scale constraint [16].

This research recommends using the I_{DDQ} scan test which typically used for the IC testing as a FA method. I_{DDQ} scan test is incorporate from the Automatic Test Pattern Generation (ATPG) method which able to stimulated limited of test vectors with higher fault coverage. This scan test is particularly to exercising the P-MOS and N-MOS transistor switching on the latches and combination logics, whereby any leaky transistor junction can be identify during the fault localization.

Failure analysis is a combination of few steps of procedure to define the possible root cause which occurs on the defective IC. The FA method may consist of combination between the testing information and appropriate diagnosis step to identify the physical defect on the IC based on the failure mode [17]. The FA method could be varies, depend on how complex the device was failed and challenge to replicate the failure mode for FA purpose.

In most events, FA becomes crucial constructive steps to translate the failure mode into an isolated area. Hereby it becomes an evolution process from the past experienced data, present use and future challenge [18].

1.2.1 Background of current FA on BCD technology.

During FA, to perform fine signal characterization on the restrict logic cell; failure analyst has to perform extra probing method on the test point besides using the external leads for voltage supply and others input/output (I/O) pins.

Typically, the test points are visible on the silicon, and they are locating at the same level as the bond pad area. The visible points are not covering by the protection layer to make it easy to contact with. The main purpose to have these test points is after the wafer fabrication process is completed, every single die inside the wafer has to undergo parametric test to validate whether it has been fabricated with correct recipe according to spec or not. This test screen at the wafer side is known as an electrical wafer sort (EWS). In this case, the numbers of test points are limited and only covering the overall parameters of the die, and not to extend until the logic cell functionality. Therefore, it is essential to have more electrical information in order to drive the defect localization during the FA works [19].

In order to overcome this challenge, failure analyst has to access underneath interconnection in order to obtain the desired signal. This signal measurement can be used by the combination between laser-cut tool and active or passive probe tip. The advantage of using probing technique is, it has to provides electrical contact directly to the restrict logic block. Commonly the desired interconnection layer are present at underneath layer where all the transistors been connected together after it been fabricated deeply in the active area [20]. Takeshi Nokuo *et al.*, (2007) and S.L Toh *et al.*, (2007), propose a conducive FA method using probing technique on nanometre device to demonstrate the probing competency.

Nevertheless, the main constraint is that not all the test points are utilize for IC diagnose in particular for scan type of failure. Even though the unforeseen underneath interconnection net is possible to reach by using probing method, uncomplimentary it may create signal distortion or interference from untested digital block inside the same IC. In few specific types of failing IC which related to the digital CMOS circuit, this method found impractical to utilize for failure analysis at all. Figure 1.2 shows the illustration of few critical points on the interconnection, concise of gap, width, and level, whereas compulsory for the probing method to obtain the signals during the failure analysis works.

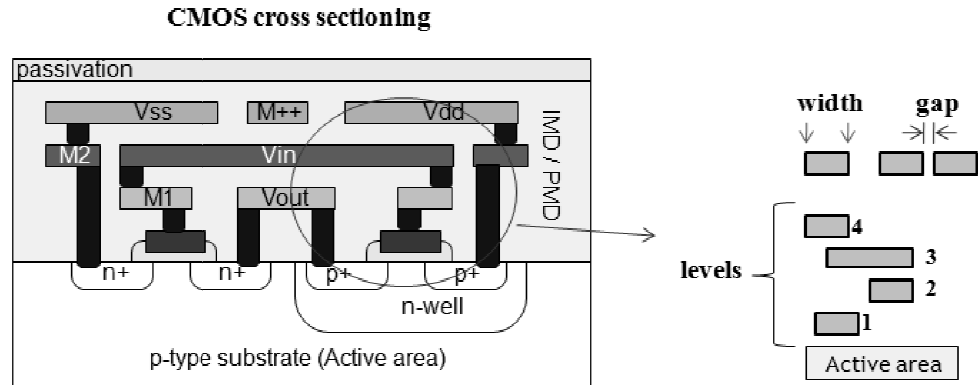


Figure 1.2: The lithography process describe the metal lines width, gap between them and space between metal layers [15].

1.2.2 Probing Method Challenge for Currently BCD FA.

For FA step using probing method, few constrain factors were identified as the metal interconnection increase on the BCD technology. In other words, this method has a tendency to cause damaged on the silicon and only limit to a few numbers of signal measurement per one time, i.e. I-V characteristic. During this step, there is a critical path that may induce damaged on the IC surface. The step begins when the probe tip starts moving from the zero position towards the desired probing points, either on the silicon or at particular underneath the metal line (after considered the top protection layer been removed using the laser-cut method).

In worst case simulation, if the probe tip has found unintentionally vibrate or wrongly positioning on the target point due to mishandling (by human factor) or vibration on probing station (by equipment stability factor), it may result of massive interconnection damaged. Figure 1.3 shows an evident in the interconnection damage result from the worst-case simulation due to mishandling event.

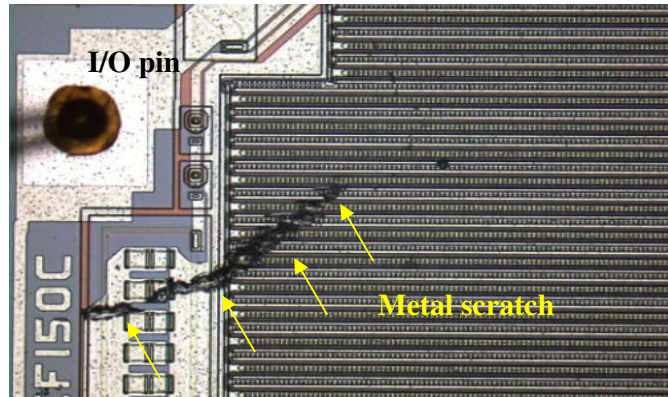


Figure 1.3: The example of damage on the silicon due to probing method [21].

As a consequence, the IC becomes malfunction by default and no longer can operate as the pre-probing step. The internal circuit of the IC probably can be either 'open' or 'short' circuit. This unforeseen circumstance becomes a fear to the analyst or FA engineer since commonly the numbers of failing sample for this specific failure mode are limited.

Another point in probing method is it only can acquire a limited number of signal measurements due to constraint between the probes versus probe point. Figure 1.4 shows the limitation on the nano-probe competency during the signal measurement on the restrict circuit. The signal measurement using limited numbers of nano-probes were only works on the desired transistor or logic circuit. Thus it is not well proficient to use in larger digital logic block [15,20].

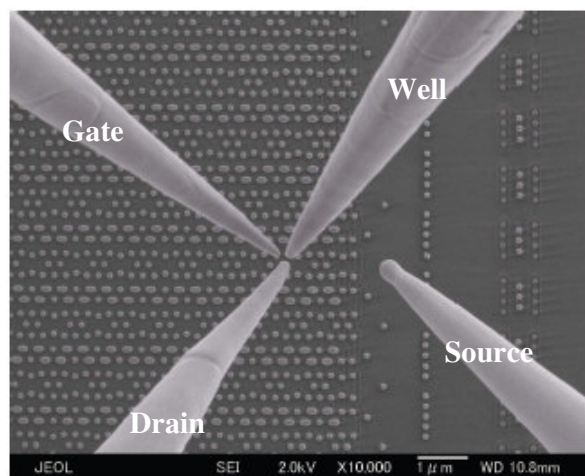


Figure 1.4: A SEM image showing four nano-probes at the source, drain, gate and well contacts of a transistor cell [20].

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