FPGA BASED MAXIMUM POWER POINT TRACKING CONTROLLER FOR PHOTOVOLTAIC SYSTEM

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ABSTRACT

Nowadays, PV cell which is known as a photovoltaic is one of the most important parts in electrical field to convert photolight to voltage and current at the desired output voltage and frequency by using varies control techniques. This project presents design and implementation of FPGA Based Maximum Power Point Tracking (MPPT) Controller for Photovoltaic system. The MPPT controller is employed to control and get Maximum Power Point (MPP) of the output voltage reference from the source. Altera DE2 board devices are used as a controller for the implementation of the MPPT system. The simulation of this FPGA based MPPT controller is designed and implemented using Quartus II VHDL software tools. The results shown, the same signal obtained from Matlab simulink software as compared with Quartus II. It has been observed that the designed system has been successfully extracting the MPP from the pseudo sources used in the simulations. The system has been evaluated in sunny day and partially shaded conditions to analyze the respective outputs in these conditions.

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LIST OF ABBREVIATIONS

AS - Active Serial

ASIC - Application Specific Integrated Circuit

CPLD - Complex Programmable Logic Device

DC - Direct Current

DSP - Digital Signal Processing

EEPROM - Electrically Erasable Programmable Read-Only Memory

FPGA - Field Programmable Gate Array

HDL - Hardware Description Language

JTAG - Joint Test Action Group

LCD - Liquid Crystal Display

LED - Light Emitting Diode

PLD - Programmable Logic Device

RAM - Random Access memory

SDRAM - Compressor-Decompressor

SOC - System On Chip

SRAM - Static Random Access memory

USB - Universal Serial Bus

VHDL - VHSIC Hardware Description Language

VHSIC - Very High Speed Integrated Circuit

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CHAPTER 1

INTRODUCTION

1.1 Project Background

Photovoltaic technology is projected to supply seventy percent of the world's energy hunger by 2030 and create a new industry far exceeding today's global automotive industry. Yes, the future for photovoltaic looks bright, global leading banks forecast a yearly growth of 25 to 35 per cent a year until 2020 and new jobs created exceeding five million globally. It is perfect time for local stakeholders to enter the burgeoning industry and establish along the PV value chain. For the industry, the race for grid when conventional electricity cost is at par with photovoltaic produced electricity cost is on. With the strong commitment from the Government of Malaysia to pursue green technologies, Malaysia is poised to play an increasingly important role in the global manufacturing of PV products benefitting the local industry.

Conventionally, the output from a PV solar cell alone is not good enough to input into an electricity bank or in to the main grid because its output is not constant in terms of voltage. This raises a need to design a controller which can calculate and extract the maximum power point at any instant from the solar cells.

Many different control strategies have already been proposed in literature such as, perturb and observe incremental conductance, parasitic capacitance, constant voltage, and artificial intelligence techniques. Conventional methods, as PID, guarantee acceptable performances, A MPPT controller is a controller that includes elements with those three functions. Whereas fuzzy logic controller (FLC) based on fuzzy logic (FL) provides a mean of converting a linguistic control strategy based on expert knowledge into an automatic strategy [1].

Field Programmable Gate Array (FPGA) based systems provide a number of run-time advantages over the sequential machines such as a microcontroller. Moreover, concurrent operations may be executed continuously and simultaneously faster than Digital Signal Processing (DSP) device. Since the functions of various components can be integrated onto the same chip, FPGAs offer lower implementation cost than DSPs that can perform only DSP-related computations. In addition, FPGAs can provide equivalent or higher performance with the customization potential of an ASIC [2]. As FPGAs can also be reprogrammed at any time, repairs can be performed in-situ while the system is running providing a high degree of robustness. Beside robustness, this re-programmability can also provide a high level of flexibility: the MPPT control system can be easily updated or modified even when it is running [2].

1.2 Problem statement

Photovoltaic (PV) is an attractive source of energy. Abundant and ubiquitous, this source is one of the most important renewable-energy sources that has been increasing worldwide year-by year. Unfortunately, PV generation systems have two major problems: -

- The conversion efficiency of electric power generation is very low (from 12% in practical generators up to a maximum of 29%) especially under low irradiation conditions.
- The amount of electric power generated by solar arrays depends on many extrinsic factors, such as irradiance (incident solar radiation) level, temperature, ageing and load conditions.

Photovoltaic technology is used to produce electricity especially in distributed renewable-energy systems. As the maximum power point (MPP) of a PV power generator depends on array temperature and irradiance, in order to maximize the energy delivered by the PV array it is necessary to track the MPP continuously.
In the last decade, several researches have focused on various MPP control algorithms to draw the maximum power of the photovoltaic array. The proposed MPPT is based on the perturbation and observation (P&O) strategy and the variable step method that control the load voltage to ensure optimal operating points of a PV system. The algorithm has been code in VHDL and realized on a generic reconfigurable architecture like FPGA. The implementation of the diagnostic algorithm on a reconfigurable architecture will make it suitable for further modification of functional logic of the processor with minimum programming effort.

1.2.1 Project Objectives

The primary objective of this project is to develop the FPGA based MPPT controller of photovoltaic system.

In addition, this project has various objectives, which comprise of:

1. To design the optimum controller by simulation for the maximum power point tracking.

2. To analyze simulations result of the maximum power point controller tracking.

3. To implement maximum power point controller on FPGA board.

1.3 Introduction of the Photovoltaic system

Photovoltaic systems are composed of interconnected components designed according to complies specific goals ranging from powering a small device to feeding electricity into the main distribution grid. Photovoltaic systems are classified according to the diagram as Figure 1.1. There are consists of two main general classifications as depicted in the Figure 1.1 which are the stand-alone and the grid-connected systems [3]. The main distinguishing factor between these two systems is that in stand-alone systems the solar energy output is matched with the load demand. The principles of operation for stand-alone is through a PV array produces power when exposed to sunlight, a number of other components are required to properly conduct, control, convert, distribute, and store the energy produced by the array. Meanwhile, it also depending on the functional and operational requirements of the system, in which the specific components required major components such as a DC-AC power inverter, battery bank, system and battery controller, auxiliary energy sources and sometimes the specified electrical load (appliances). Figure 1.2 shows a basic diagram of a photovoltaic system and the relationship of individual components.

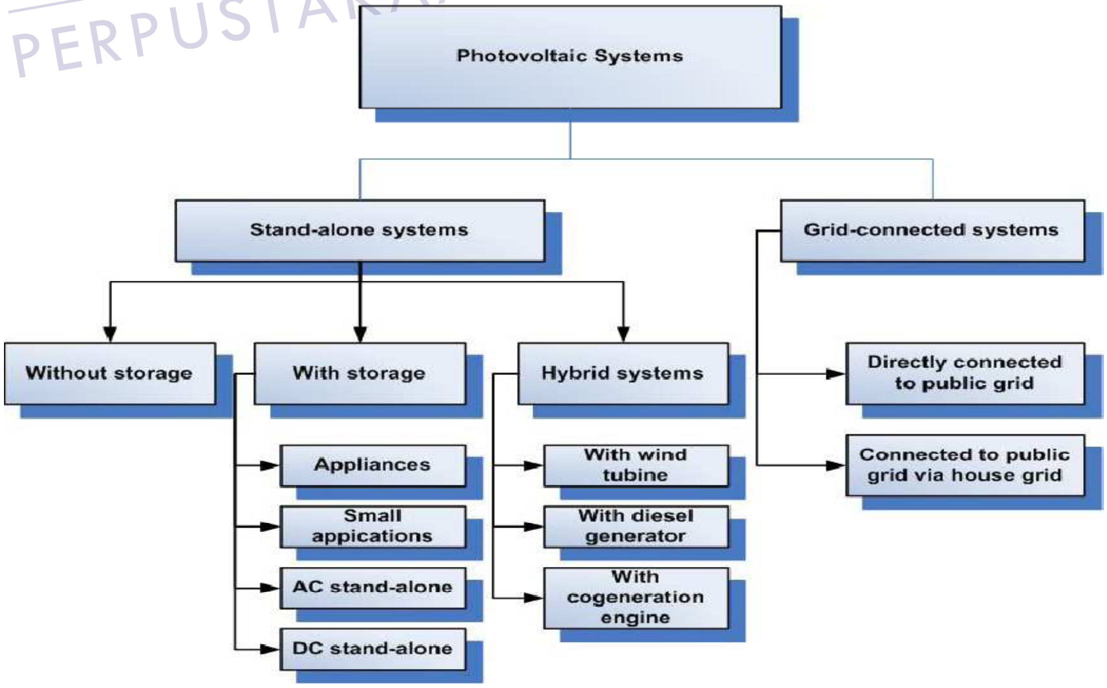

Figure 1.1: Classification of PV systems

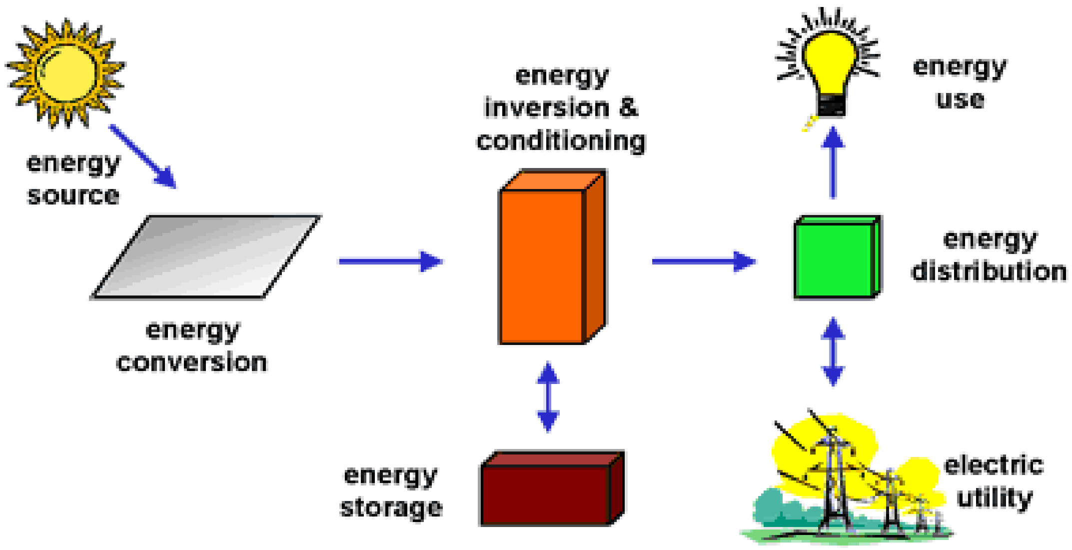

Figure 1.2: Stand alone PV systems with load

1.4 Maximum Power Point Tracking (MPPT)

It is evident that the output characteristics of the PV panel are non-linear in nature and vary with atmospheric conditions namely temperature, irradiance and etc. Tracking the maximum power point (MPP) of a photovoltaic (PV) array is usually an essential part of a PV system. As such, many MPP tracking (MPPT) methods have been developed and implemented [1-4]. An MPPT is a control algorithm that can be included in the PV panel connections in order to track the maximum power point, which is going to be different from the STC (Standard Test Conditions) rating under almost all situations [5]. MPPT Algorithms can be basically classified into two categories On-line and Off-line methods. On-line methods measure operating voltage and/or current and compare the present value of power with the previously obtained values and appropriate changes in the reference value are made so as to cause a further increase in power ultimately tracking the operating point that operates at maximum power. Online methods are usually more expensive due to extra circuitry employed and are usually only used in large PV systems[6]. However, with the availability of low-cost based microcontrollers and field programmable gate arrays (FPGAs) these methods can also be applicable to module based power electronic interfaces. Off-line methods rely on the measurement of parameters like irradiance, panel temperature, short circuit current, open circuit voltage of the PV array, Which the use of prior training data to set the reference signal corresponding to operation at the maximum power point (MPP). This methods present reduced implementation costs, but sub-optimum performance [7-9]. Fuzzy logic is being increasingly used in present times as a convenient tool to model and control systems, which are nonlinear in nature, the solar PV array being no exception. In this project we use a P&O and Fuzzy logic based controller along with instantaneous values of PV voltage and current and peak current control for determining not only the direction of the next perturbation (variation of reference current) but also its magnitude, by which one can enhance both transient and steady-state operation simultaneously.

1.5 VHDL Programming

VHDL stands for VHSIC Hardware description Language. VHSIC means Very High Speed Integrated Circuit. VHDL is a hardware description language which describes the behavior of an electronic circuit or system from which the physical circuit or system can be attained of implemented. This hardware description language has become popular nowadays in the electronics design community due to its ability to easily migrate code from one system to another. Since a VHDL design is just a text file, it can be used with a wide variety of software tools without worrying about data compatibility. VHDL is a computer language used to model and synthesize digital hardware. As its title implies, VHDL is used to describe the structure or behavior of hardware, and then determine how it should operate (modeling) or how it should be built (synthesis). A programmer enters text according to the syntax of language, then use appropriate software to compile, simulate and synthesize the design [10].

1.6 Finite State Machine Design Using VHDL

Finite state machines (FSMs) are generally used as controllers in digital designs. Until now, probably some people have designed quite a few state machines on paper, but there was no real point for the design. But up to the point where these designs still don't have much point but it is possible to be able to implement and test them using actual hardware. The first step in this process is to learn how to model FSMs using VHDL. As illustrated in Figure 1.3, simple FSM designs are just a step beyond the sequential circuits described in the section dealing with memory elements in VHDL. The techniques discussed in this section will allow to quickly and easily designing relatively complex FSMs which can be used as controllers in digital circuits. A block diagram for a standard Moore-type FSM is shown in Figure 1.3. This diagram looks fairly typical but some different names are used for the some of the blocks in the design. The *Next State Decoder* is a block of combinatorial logic that uses the current external inputs and the current state of the FSM to decide upon the next state of the FSM. In other words, the inputs to the Next State Decoder block are decoded and to produce an output that represents the next state of the FSM. The circuitry in Next State Decoder is generally the excitation equations for the storage elements (flip-flops) in the State Register block. The next state becomes the present state of the FSM when the clock input to the *state registers* block becomes active. The state registers block is storage elements that store the present state of the machine. The inputs to the *Output Decoder* are used to generate the desired external outputs. The inputs are decoder via combinatorial logic to produce the external outputs. Because the external outputs are only dependent upon the current state of the machine, this FSM is classified as a Moore FSM [11].

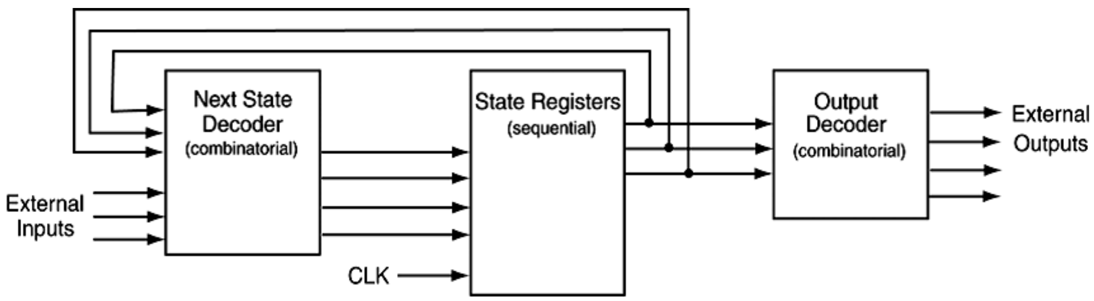

Figure 1.3: Block diagram for a Moore-type FSM.

The FSM model shown in Figure 1.3 is probably the model of a Moore-type FSM. Most commonly FSM are required to generate the combinatorial logic required to implement the next state decoder and the output decoder. But here FSMs discussed in the context of VHDL. The true power of VHDL starts to emerge in its dealings with FSMs. the versatility of VHDL behavioral modeling removes the need for large paper designs of endless K-maps and endless combinatorial logic. There are several different approaches used to model FSMs using VHDL. The many different possible approaches are the result of the general versatility of VHDL as a programming language. This section discuses the probability of the clearest approach for FSM implementation. A block diagram of the approach used in the implementation of FSMs is shown in Figure 1.4. The approach used here divides the FSM into two VHDL processes. One process, referred to as the *Synchronous Process*, handles all the matters regarding clocking and other controls associated with the storage element. The other process, the *Combinatorial* handles all the matters associated with the Next State Decoder and the Output Decoder of Figure 1.3. Note that the two blocks in Figure 1.3 are both comprised of solely of combinatorial logic. There is some new lingo used in the description of signals used in Figure 1.4 this description is outlined and described below:

- The inputs labeled *Parallel Inputs* are used to signify inputs that act in parallel to each of the storage elements. These inputs would include enables, presets, clears, etc.
- The inputs labeled *State Transition Inputs* include external inputs that control state transitions. These inputs also include external inputs used to decode Mealy-type external outputs.
- The *Present State* signals are used by the Combinatorial Process box for both next state decoding and output decoding. The diagram of Figure 1.4 also shows that the Present State variables can also be provided as outputs to the FSM but is not required.

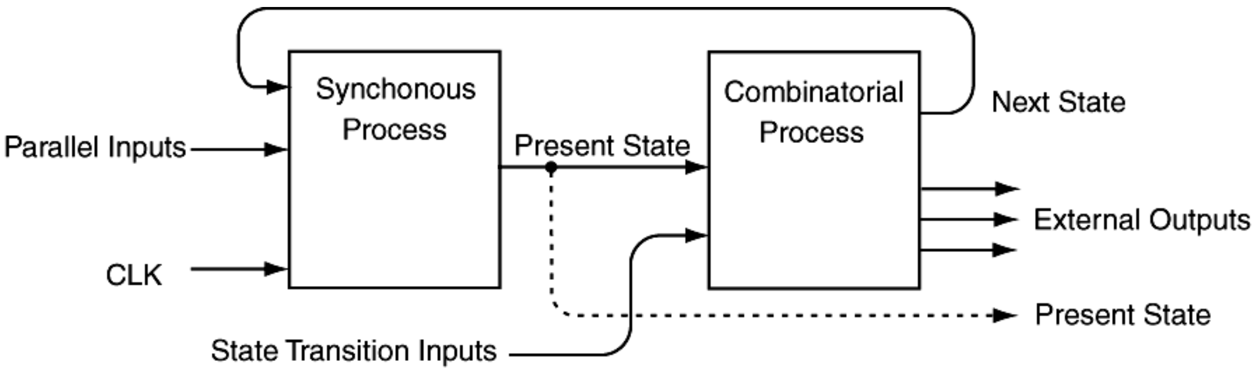

Figure 1.4: Model for VHDL implementations of FSMs.

Although there are many different methods that can be used to described FSMs using VHDL, two of the more common approaches are the *dependent* and *independent PS/NS* styles. Only the dependent style is covered in this study because it is clearer than the independent PS/NS style [11]. The model shown in Figure 1.4 is actually a model of the dependent PS/NS style of FSMs.

CHAPTER 2

LITERATURE REVIEW

2.1 Introduction

This chapter is about the discussion of all the summarized information of the relevant studies to implement FPGA on designing the MPPT method for PV system, including VHDL programming, Field Programmable Gate Array (FPGA) and the features of Altera DE2 board. Furthermore, this chapter are also discussing about a study on the previous research based on journals and conferences. The sources of the literatures review are from journals, conferences and books.

2.2 Photovoltaic performance

The amount of power generated from a photovoltaic (PV) system mainly depends on the following factors, such as temperatures and solar irradiances. According to the high cost and low efficiency of a PV system, it should be operated at the maximum power point (MPP) which changes with solar irradiances or load variations.

2.2.1 PV characteristics

There are three classic parameters that are very important on the PV characteristics namely short-circuit current (I_{sc}), open-circuit voltage (V_{oc}) and the maximum power point (I_{mp};V_{mp}). The power delivered by a PV cell attains a maximum value at the points (I_{mp};V_{mp}). The short circuit current is measured by shorting the output terminals and measuring the terminal current [3].

2.2.1.1 Maximum Power (P_{MAX}), Current at P_{MAX} (I_{MP}), Voltage at P_{MAX} (V_{MP})

The power produced by the cell in Watts can be easily calculated along the I-V sweep by the equation $P=IV$. At the I_{SC} and V_{OC} points, the maximum value for power will occur between the two. The voltage and current at this maximum power point are denoted as V_{MP} and I_{MP} respectively. The Figure 2.1 is interpreted the Maximum Power for an I-V curve.

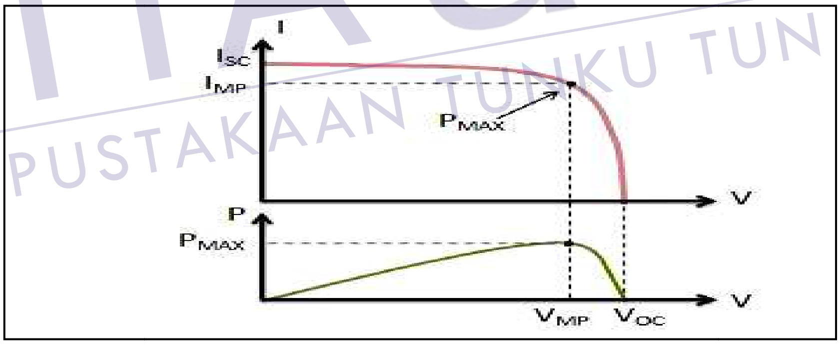

Figure 2.1: Maximum Power for an I-V curve

By taking the absolute air mass (AM_a) function is equal to 1.0 and combining the beam and diffuse component into single component of irradiance, the short circuit can be obtained as below:

$$I_{sc=}I_{sco}E_e\,(1 + a_{Isc}(T_c - T_0)) \tag{2.1}$$

The open circuit voltage (V_{oc}), the maximum power point current (I_{mp}) and maximum power point voltage (V_{mp}) can be defined as below:

$$V_{oc} = V_{oco} + N_s\delta(T_c) + In(E_e) + \beta_{Voco}E_e(T_c - T_0) \tag{2.2}$$

$$I_{mp} = I_{mpo}(C_o E_e + C_1 E_1^2)\,(1 + \alpha_{Imp}(T_c - T_0)) \tag{2.3}$$

$$V_{mp} = V_{mpo} + C_2 N_s \delta(T_c) In(E_e) C_3 N_3 (\delta(T_c) \text{In}\,(E_e))^2 + \beta_{Voco} E_e (T_c - T_0) \tag{2.4}$$

2.2.1.1.1 Nomenclature

E	Irradiance level on module surface, W/m^2
E_e	Effective irradiance or "Suns"
AM_a	Absolute air mass (dimensionless)
AOI	Angle of incident (degree)
T_c, T_0	Cell and reference temperature (degree Celsius)
I_{sco}, I_{mpo}	Short circuit current and current at MPP at STC
V_{sco}, V_{mpo}	Open circuit voltage and voltage at MPP at STC
$a_{Isc}, a_{Imp}, \beta_{Voco}, \beta_{Vmpo}$	Normalized temperature coefficients
C_0-C_3	Empirically determined coefficients
N_s	Number of cells in series
STC	$\mathrm{E{=}1000\ W/m^2,\ \ T_c{=}25C^0, AM_0 = 1.5, AOI = 0^0}$

2.2.1.2 Fill Factor (FF)

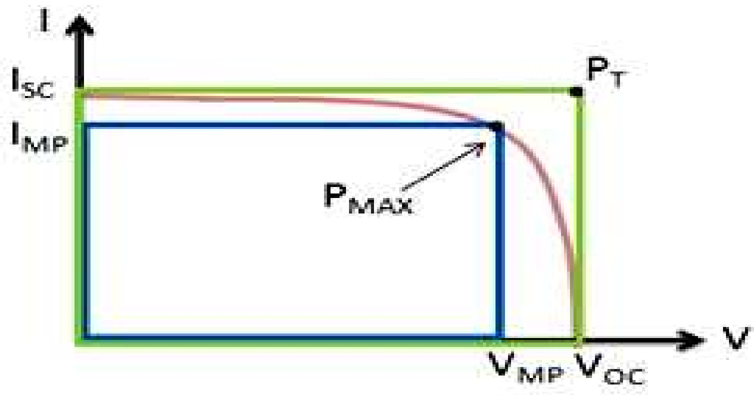

Figure 2.2: Photovoltaic module characteristics showing the Fill Factor

Another important parameter of the PV characteristics is called the Fill Factor (FF) is shown in Figure 2.2. It is a term that describes how the curve fills the rectangle that is defined by (Voc) and (Isc). It gives an indication of the quality of a cell's semiconductor junction and measures of how well a solar cell is able to collect the carriers generated by light [3]. It is defined as:

$$F = \frac{V_{mpp}I_{mpp}}{V_{oc}I_{oc}} \tag{2.5}$$

After a simple manipulation the following equation results:

$$V_{oc}I_{oc} \times FF = V_{mpp}I_{mpp}=P_{max} \tag{2.6}$$

Those parameters are strongly depending the effect of cell temperatures and the irradiance that produced by sunlight.

2.3 PV materials

PV cells are made of semiconductor materials with crystalline and thin films being the dominant materials. The majority of PV-cells are silicon-based but in the near future other thin film materials are likely going to surpass silicon PV cells in terms of cost and performance [12]. PV materials may fall into one or more of the following classes: crystalline, thin film, amorphous, multi-junction, organic or photochemical. In this project,150 Watt Multi-crystalline photovoltaic module with Poly-crystalline silicon technology, namely BPSX150. Table 1 describe its characteristics.

Table 1: Typical Electrical of BP SX -150

Electric parameter	**BPSX150**
Maximum power, P_{max}	150 W
Maximum current (short circuit output), I_{mp}	4.35 A
Maximum voltage (open circuit), V_{mp}	34.5 V
Short circuit current, I_{sc}	4.75 A
Open circuit voltage, V_{sc}	43.5 V
NOCT 2) [°C]	47 ±2°C
Temp. coefficient: short-circuit current	(0.065±0.015)%/°C
Temp. coefficient: open-circuit voltage	–(160±20)mV/°C

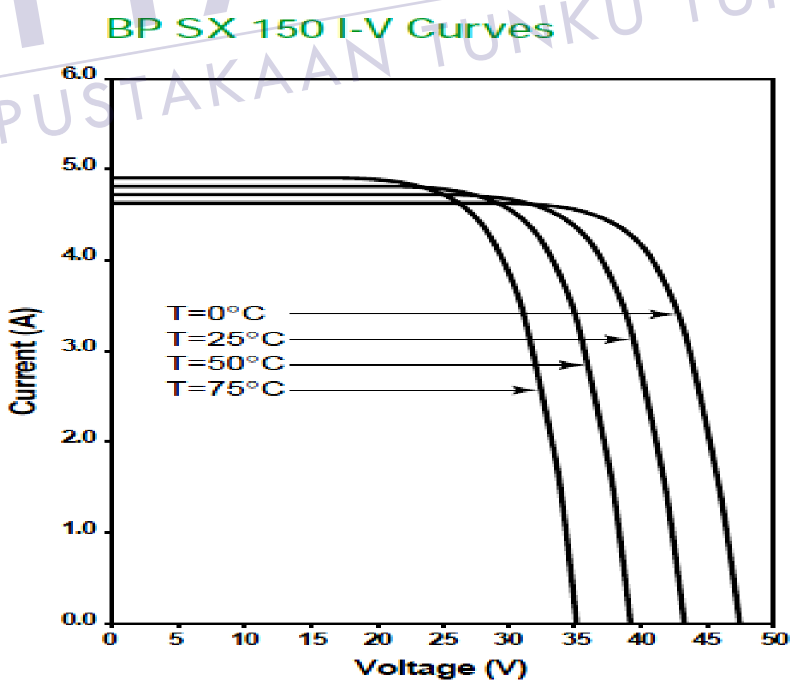

Figure 2.3: BP SX 150 I-V Curves

2.3.1 Crystalline materials

2.3.1.1 Single-crystal silicon

Mono-crystalline silicon cells have in the past dominated the PV market but have now been overtaken by poly-crystalline silicon. The popularity of mono-crystalline silicon was due to the good stability and desirable electronic, physical and chemical properties of silicon. Moreover, silicon was already successful in microelectronics and the enormous industry thus created would benefit the smaller PV industry with regards to economy of scale [13].

2.3.1.2 Poly-crystalline silicon

This is the currently most dominant material and has surpassed the mono-crystalline because it is cheaper. The cost of silicon is a significant portion of the cost of the solar cell. The manufacturing processes of poly-crystalline silicon reduces the cost of silicon by avoiding pulling in the manufacturing process and it results in a block with a large crystal grain structure. This results in cheaper cells with a somewhat lower efficiency. The assembly of multi-crystal wafers is easier and therefore offsets the low efficiency disadvantage [14].

2.4 MPPT Algorithms

All the MPPT algorithms are designed to dynamically extract the maximum power from the PV panels. Usually, the condition $\partial p/\partial v = 0$ is adopted to locate this operating point, since PV panels show a unique global maximum power point. The MPPT algorithms are based on the determination of the slope of the PV panel's output power versus voltage, i.e., the power derivative $\partial p/\partial v$. This quantity is utilized as representative of the "voltage error", i.e., the difference between the actual voltage of the PV panels and the reference voltage v^* corresponding to the maximum power operating point. The qualitative behavior of $\partial p/\partial v$ is represented in Figure 2.4. In the region nearby v^* the power derivative can be considered a straight line having the slope k. In order to determine the power derivative $\partial p/\partial v$ it is necessary to introduce a voltage and current perturbation around any operating point of the PV array. Traditional MPPT algorithms are based on “perturbation and observation” method or “incremental conductance” method [15].

Among these techniques, the P&O and the incremental conductance algorithms are the most common. These techniques have the advantage of an easy implementation but they also have drawbacks, as will be shown later. In normal conditions the V-P curve has only one maximum, so it is not a problem. However, if the PV array is partially shaded, there are multiple maxima in these curves. In order to relieve this problem, some algorithms have been implemented as in [14]. In the next section the most popular MPPT techniques are discussed [16].

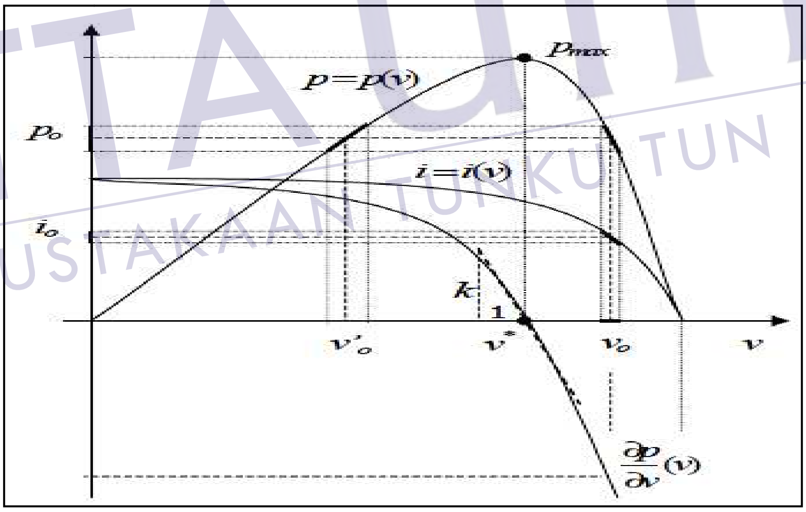

Figure 2.4: Current, power, and power derivative of the PV panels vs. voltage

2.4.1 Perturb and Observe

The concept behind the "perturb and observe" (P&O) method is to modify the operating voltage or current of the photovoltaic panel until you obtain maximum power from it. For example, if increasing the voltage to a panel increases the power output of the panel, the system continues increasing the operating voltage until the power output begins to decrease. Once this happens, the voltage is decreased to get back towards the maximum power point. This perturbation continues indefinitely. Thus, the power output value oscillates around a maximum power point and never stabilizes [16].

P&O is simple to implement and thus can be implemented quickly. The major drawbacks of the P&O method are that the power obtained oscillates around the maximum power point in steady state operation. It can track in the wrong direction under rapidly varying irradiance levels and load levels, and the step size (the magnitude of the change in the operating voltage) determines both the speed of convergence to the MPP and the range of oscillation around the MPP at steady state operation [17]. The operation of a P&O MPPT is as shown in the Figure 2.5. where any V_k and I_k are the actual voltage and current , whereas V_{k-1} and I_{k-1} are the previous state for voltage and current.

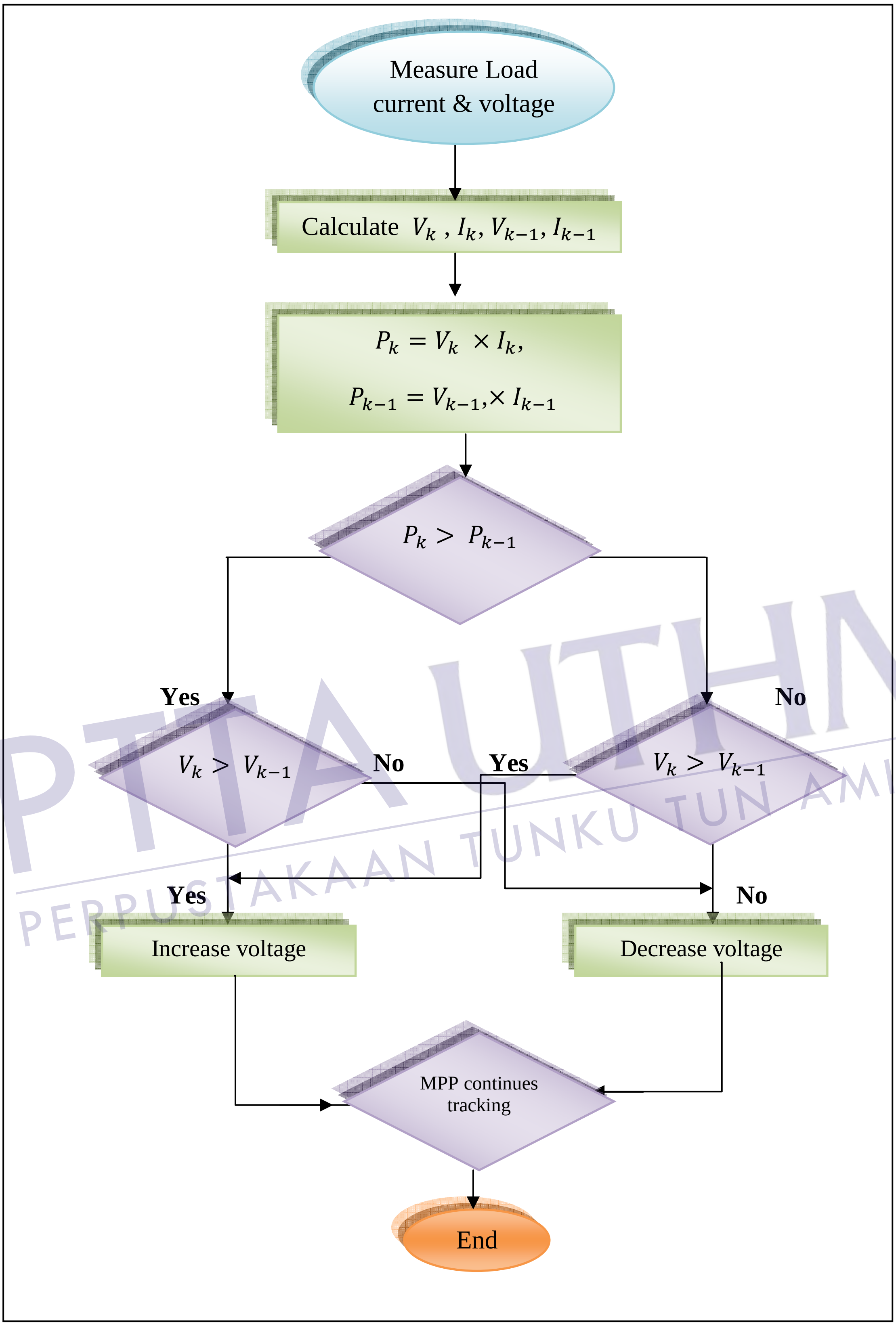

Figure 2.5: P&O MPPT operation Flow Chart

2.4.2 Constant Conductance

Constant conductance considers the fact that the slope of the power-voltage curve is zero at the maximum power point, positive at the left of the MPP, and negative at the right of the MPP. The MPP is found by comparing the instantaneous conductance (I/V) to the incremental conductance (ΔI/ΔV)[18] .This algorithm is based on the principle that at the MPP $\partial p/\partial v = 0$, and as $p = IV$, it yields

$$\begin{cases} \partial p/\partial V = 0 \quad at\ V = Vmp \\ \partial p/\partial V > 0 \quad at\ V < Vmp \\ \partial p/\partial V < 0 \quad at\ V > Vmp \end{cases} \tag{2.7}$$

A scheme of the algorithm is shown in Figure 2.6. Similar schemes can be found in [9].

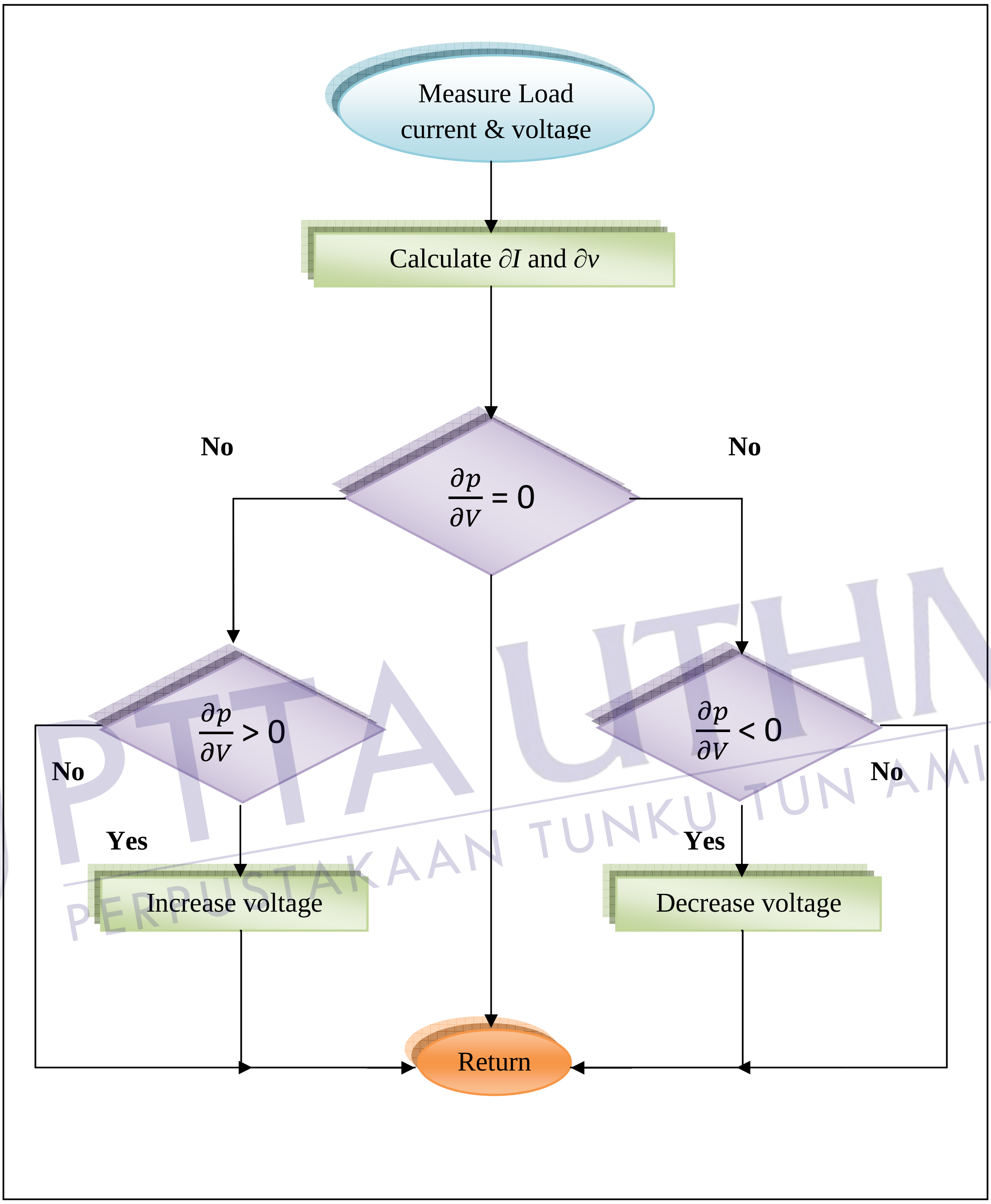

Figure 2.6: Constant conductance MPPT operation Flow Chart

By comparing the increment of the power vs. the increment of the voltage (current) between two consecutives samples, the change in the MPP voltage can be determined. In addition, S is defined, as the sum of the array incremental and instantaneous conductance. Thus,

$$S = \frac{dI}{dV} + \frac{I}{V} \tag{2.8}$$

At the MPP, $\partial p/\partial v = 0$, can be rewritten as

$$S = 0 \tag{2.9}$$

which can be taken as the desired input (i.e. set-point) for the suggested control system.

The task of the MPPT algorithm is to calculate the reference voltage (Vref) towards which the PV operating voltage should move next for obtaining maximum power output.

To offer a reasonable comparison of these approaches with the approach proposed in this thesis, a set of criteria is put forth to motivate the comparison. This set consists of the following criteria:

(i) *Cost*: How far does an MPPT design meet the low cost constraints demanded in the commercial market? The penetration of MPPT control technologies in this market depends heavily on their cost.

(ii) *Performance*: What performance is the MPPT design capable of providing? Future control applications may require nimble and swift power control.

(iii) *Robustness*: Is the MPPT design capable of operating in a wide range of environmental conditions such as noisy environments? Robustness is highly valued in the commercial market.

(iv) *Flexibility*: Can the MPPT design be easily upgraded or modified to meet a new design constraint? New efforts of research and development may require the design to be quickly and easily modified.

(v) *Expandability*: Can the MPPT design be expanded to accommodate increasing control requirements? It is anticipated that future MPP control systems will require handling of multi-channels.

(vi) *Testability*: Can the MPPT design be easily tested, verified, and validated against a set of requirements? The commercial market is highly aware that testability has a significant impact on cost.

The remaining chapters in this thesis present a design which is based on a popular MPPT algorithm and is highly suitable for a commercial market given its cost savings, its robustness, its flexibility, and its expandability to handle multi-channel control [19].

2.5 Field Programmable Gate Array (FPGA)

A Field-Programmable Gate Array (FPGA) is an integrated circuit designed to be configured by the customer or designer after manufacturing. FPGA are programmed using a logic circuit diagram or a source code in a Hardware Description Language (HDL) to specify how the chip will operate. Previously, the Application-Specific Integrated Circuit (ASIC) in circuit diagrams form is used to specify the configuration. A combination of volume, fabrication improvements, research and development, and the I/O capabilities of new supercomputers have largely closed the performance gap between ASICs and FPGAs. FPGAs originally began as competitors to CPLDs (Complex Programmable Logic Device). As their size, capabilities, and speed increased, FPGAs began to take over larger and larger functions to the state where some are now marketed as full Systems on Chips (SoC) [20]. Applications of FPGAs include digital signal processing, software-defined radio, aerospace and defense systems, ASIC prototyping, medical imaging, computer vision, speech recognition, cryptography, bioinformatics, computer hardware emulation, radio astronomy, metal detection and a growing range of other areas. FPGAs are increasingly used in conventional high performance computing applications where computational kernels such as FFT or Convolution are performed on the FPGA instead of a microprocessor.

2.5.1. FPGA Architectures

Table 2: FPGA Technologies type and companies

Company	Low-cost FPGA	High-density FPGA	FPGA with embedded processors, DSP and transceivers	FPGA with More DSP and LUT6	Latest
Altera	Cyclone	Stratix	Stratix GX, Excalibur	Stratix IV, Cyclone III	Stratix V Cyclone V
Xilinx	Spartan	Virtex	Virtex II Pro, Virtex 4, Virtex5 (LUT6)	Virtex 6, Spartan 6	Virtex 7 Kintex 7 Artix7

2.5.2. ALTERA Technology

Altera Corporation is a Silicon Valley manufacturer of PLDs, reconfigurable complex digital circuits. The company released its first PLD in 1984. Altera's main products are the Stratix, Arria and Cyclone series FPGAs,[2] the MAX series CPLDs (Complex programmable logic devices),[2] the HardCopy series ASICs and Quartus II design software [21].

The Stratix and Cyclone series FPGAs are the company's largest, highest bandwidth devices, with up to 1.1 million logic elements, integrated transceivers at up to 28 Gbit/s, up to 1.6 Tbit/s of serial switching capability, up to 1,840 GMACs of signal-processing performance, and up to 7 x72 DDR3 memory interfaces at 800 MHz. Cyclone series FPGAs and SoC FPGAs are the company's lowest cost, lowest power FPGAs, with variants offering integrated transceivers up to 5 Gbit/s. In between these two device families are Arria series FPGAs and SoC FPGAs, which provide a balance of performance, power, and cost for mid-range applications such as remote radio heads, video conferencing equipment, and wireline access equipment. Arria

FPGAs have integrated transceivers up to 10 Gbit/s. Altera's largest competitor and long-time rival is FPGA founder and market-share leader Xilinx [22]. The next closest competitor is Lattice Semiconductor, representing less than 10 percent of the market [22]. Other FPGA makers, Actel (now Microsemi) and QuickLogic, sell to differentiated market segments that Altera mostly does not address.

In broader terms, Altera competes with ASIC, Structured ASIC, and Zero Mask-Charge ASIC companies like eASIC. Moore's Law and improving software tools are rapidly expanding FPGAs' potential markets.

2.5.2.1 ALTERA DE2 board

The Altera DE2 board has many features that allow the user to implement a wide range of designed circuits, from simple circuits to various multimedia projects. A photograph of the DE2 board is shown in Figure 2.7. It depicts the layout of the board and indicates the location of the connectors and key components. In order to use the DE2 board, the user has to be familiar with the Quartus II software.

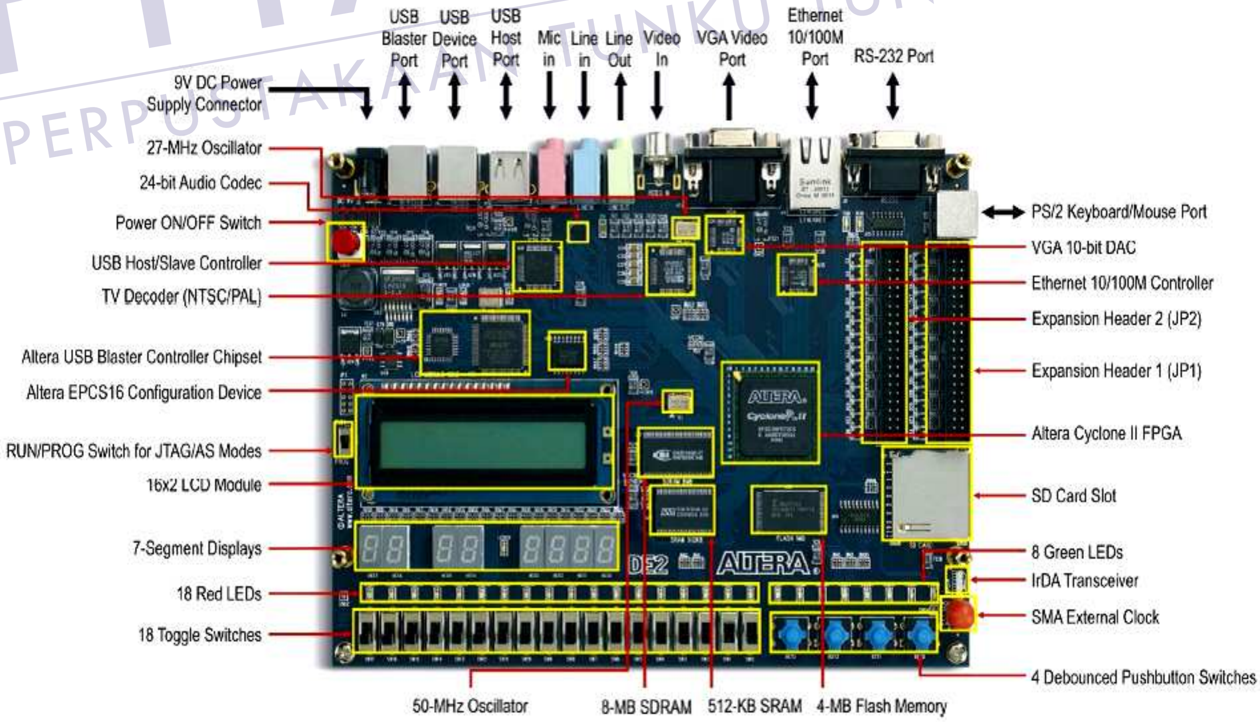

Figure 2.7: ALTERA DE2-Cyclone II EP2C35F672C6 board (Adapted from Altera.com)

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