SIMULATION, FABRICATION AND CHARACTERIZATION OF PMOS TRANSISTOR DEVICE

SITI IDZURA BINTI YUSUF

KOLEJ UNIVERSITI TEKNOLOGI TUN HUSSEIN ONN

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Alamat Tetap:

PEJABAT LADANG FELDA LEPAR UTARA 13,
WAKIL POS LEPAR UTARA 1,
84300 BANDAR PUSAT JENGKA,
PAHANG

PROF. Dr. HASHIM BIN SAIM

Nama Penyelia

Tarikh: 21 DISEMBER 2006

Tarikh: 21 DISEMBER 2006

CATATAN:

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SITI IDZURA BINTI YUSUF

This thesis is submitted in partial to fulfillment of the requirement for the Master of Electrical Engineering

Faculty of Electrical And Electronic Engineering
Tun Hussien Onn University College of Technology

DECEMBER, 2006

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Name of Student : SITI IDZURA BINTI YUSUF

Date : 21 DECEMBER 2006

Khas buat tunang Muhammad Syukur Bin Ismail

Setiap kejayaanku milik kita bersama

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ABSTRACT

In a low supply voltage CMOS technology, it is desirable to scale threshold voltage and gate length for improving circuit performance. Therefore, a project has been carried out inside KUiTTHO's microelectronic cleanroom to produce a method that has better low power/low voltage current concentrate on p-channel (PMOS). An experiment was also done to determine the right parameter value to be used for fabrication process such as oxidation process thickness rate, sheet resistance and metal thickness. From the parameter value obtained, 0.3 mm and 0.5 mm PMOS transistor had been successfully produced. Fabrication simulation was performed to produce a 0.1μm and 0.3μm PMOS transistor by using the ISE-TCAD software. The trade off between threshold voltage (V_{TH}), gate length (L_G) and thin oxide thickness (t_{ox}) are discussed to determine the characteristics of the transistors. It shows that for 0.3mm (t_{ox} = 860Å) PMOS transistor the value of V_{TH} =-3.33V and 0.5 mm (t_{ox} = 910Å), V_{TH} value =-4.3V. From the simulation result show for 0.1μm (t_{ox} = 200Å), V_{TH} = -0.314V and for 0.5μm (400Å) V_{TH} = -0.634V. The result shows that, with decreasing gate length and oxide thickness will produce lower value of threshold voltage. Minimum value of threshold voltage can result in a better performance of transistor. Another parameter must be taken into consideration such as leakage current, resistivity and conductivity to get a better design of PMOS transistor in future research.

ABSTRAK

Untuk menghasilkan sumber voltan yang rendah dalam CMOS teknologi, penskalaan voltan ambang, V_{TH} dan lebar gate, L_G untuk menghasilkan litar yang berkeupayaan tinggi ,merupakan isue yang sangat penting. Oleh itu, projek ini telah dijalankan di dalam makmal mikroelektronik bilik bersih KUiTTHO untuk menghasilkan resepi bagi PMOS transistor dengan saiz yang minimum dan berprestasi tinggi. Eksperimen juga telah dijalankan untuk menentukan nilai parameter yang sesuai untuk digunakan dalam proses fabrikasi iaitu proses pengoksidaan untuk mencari kadar ketebalan oksida get, rintangan keping dan ketebalan metal. Daripada nilai parameter yang diperolehi, 0.3mm dan 0.5mm PMOS transistor telah berjaya dihasilkan. Fabrikasi secara simulasi juga telah dijalankan untuk menghasilkan 0.1μm and 0.3μm PMOS transistor dengan menggunakan perisian ISE-TCAD. Perubahan antara voltan ambang (V_{TH}), lebar gate (L_G) dan ketebalan lapisan oksida (t_{ox}) telah dibincangkan untuk menetukan ciri-ciri bagi PMOS transistor tersebut. Hasil dapat daripada fabrikasi sebenar menunjukkan untuk transistor bersaiz 0.3mm (t_{ox}= 860Å) PMOS transistor V_{TH} = -3.33V dan 0.5mm(t_{ox} = 910 Å), nilai V_{TH} = -4.3V. Dapatan hasil simulasi menunjukkan untuk 0.1μm (t_{ox} = 200Å), V_{TH} = -0.314V dan 0.5μm (t_{ox} = 400Å), nilai V_{TH} = -0.634V. Daripada keputusan yang diperolehi menunjukkan bahawa dengan kelebaran get yang minima dan ketebalan oksida yang lebih nipis akan menghasilkan PMOS transistor dengan nilai voltan ambang yang lebih rendah. Nilai voltan ambang yang lebih rendah akan mempengaruhi keupayaan transistor. Parameter-parameter lain perlu diambil kira seperti arus bocor, kerintangan dan kekonduksian untuk menghasilkan PMOS transistor yang berprestasi tinggi untuk kajian akan datang.

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LIST OF SYMBOLS / ABBREVATIONS

Å	symbol for 10^{-10}cm or 10^{-8}m
C	Capacitance
C_{ox}	Oxide capacitance per unit area
D	Diffusion coefficient
I	Current
I_D	Drain current
I_D-V_D	Drain Current versus Drain / source Voltage
k	Boltzmann's constant
L	Length
L_G	Gate Length
n	Electron density
n_i	Intrinsic carrier density
N	Doping density
N_a	Acceptor doping density
N_c	Effective density of states in the conduction band
N_d	Donor doping density
R	Resistance
R_s	Sheet Resistance
S_i	Silicon
t	Thickness
t_{ox}	Oxide thickness
T	Temperature
v	Velocity

V_D	Drain voltage
V_{DS}	Voltage gate to source
V_B	Body voltage
V_G	Gate voltage
V_{GS}	Voltage gate to source
V_{TH}	Threshold voltage
W	Width
x_d	Depletion layer width
xj	Junction depth
x_n	Depletion layer width in an n-type semiconductor
μ_p	Hole mobility

CHAPTER I

INTRODUCTION

1.1 General

The MOSFET circuit technology has dramatically changed over the last three decades. Starting with a ten-micron PMOS process with an aluminum gate and a single metallization layer around 1970, the technology has evolved into a tenth-micron self-aligned-gate CMOS process with up to five metallization levels. The transition from dopant diffusion to ion implantation, from thermal oxidation to oxide deposition, from a metal gate to a poly-silicon gate, from wet chemical etching to dry etching and more recently from aluminum (with 2% copper) wiring to copper wiring has provided vastly superior analog and digital CMOS circuits. The choice and centering of target transistor parameters- modeling (such as threshold voltage, gate length, gate oxide thickness, etc) for high speed low-power/ low voltage CMOS technologies is a current concern (Chang, 2000)[7]. If proper CMOS scaling rules are utilized, high speed CMOS technologies can be achieved even in conjunction with reduced supply voltage requirements. The dynamic power dissipation in CMOS inverter circuits is given by

$$P = f.C_L.V^2_D \quad (1.1)$$

where f is operating frequency, C_L is the loading capacitance, and V_D is the supply voltage. Clearly, reducing the supply voltage is the simplest approach in reducing the dynamic power consumption. The time delay, τ_D in a CMOS gate is approximately given by

$$\tau_D \approx \frac{C_L V_D}{I_D} \infty \frac{C_L L_G t_{ox} V_D}{(V_D - V_{TH})^2} \quad (1.2)$$

where L_G is the transistor gate length, t_{ox} is the gate oxide thickness, I_D drain current and V_{TH} is the MOS transistor threshold voltage. Equation 1.2 demonstrates the need for reducing the gate oxide thickness, the gate length, and the transistor threshold voltage in order to preserve the high-speed in a reduced voltage supply technology.

1.2 Problem Statement

Since the semiconductor industry growth rapidly, competition among companies to fulfill market demands has become increasingly intense. Therefore, many data and parameters obtained from researches were not published and kept confidential. Hence, each fabrication laboratories have created their own technologies. KUiTTHO as an education institution is also making an effort to produce a MOSFET technology transistor with the equipment provided in the KUiTTHO's Microelectronic Cleanroom. Therefore, the purpose of this project was to build a first MOSFET technology transistor, which was aimed for better low power/low voltage current concentrate on p-channel (PMOS) transistors.

1.3 Project Objectives

The objectives of this project are:

1. To produce a recipe of MOSFET devices (PMOS transistor).
2. To determine the minimum mask design that can be fabricated in KUiTTHO's cleanroom to produce transistor with minimum gate length.
3. To determine transistor region operation which are very important in low-voltage and low-power application from the IV characteristics of PMOS transistor.
4. To determine the trade-off between threshold voltage (V_{TH}) and the minimum gate length (L_G) for optimizing the performance of PMOS transistors for low voltage/low power high-speed digital CMOS circuit.

1.4 Project Scope

1. The project was done with the process equipments in Microelctronic Cleanroom at KUiTTHO. The data that was obtained might be different with other clean-room. It depends on the equipment capability and the class of the cleanroom.
2. The project concentrated on PMOS transistor device, including the effect of threshold voltage(V_{TH}) thin oxide thickness (t_{ox}) and gate length (L_G) to I_D-V_D characteristics.
3. There were 4 steps that were taken in this project which were:
    i. Establishing process module, process parameters, process flow and process run card.
    ii. Optimizing and characterizing process module.

iii. Integrating the process module and starting the fabrication process of MOSFET (PMOS) device.

iv. Analyzing and testing product.

1.5 Project Flow

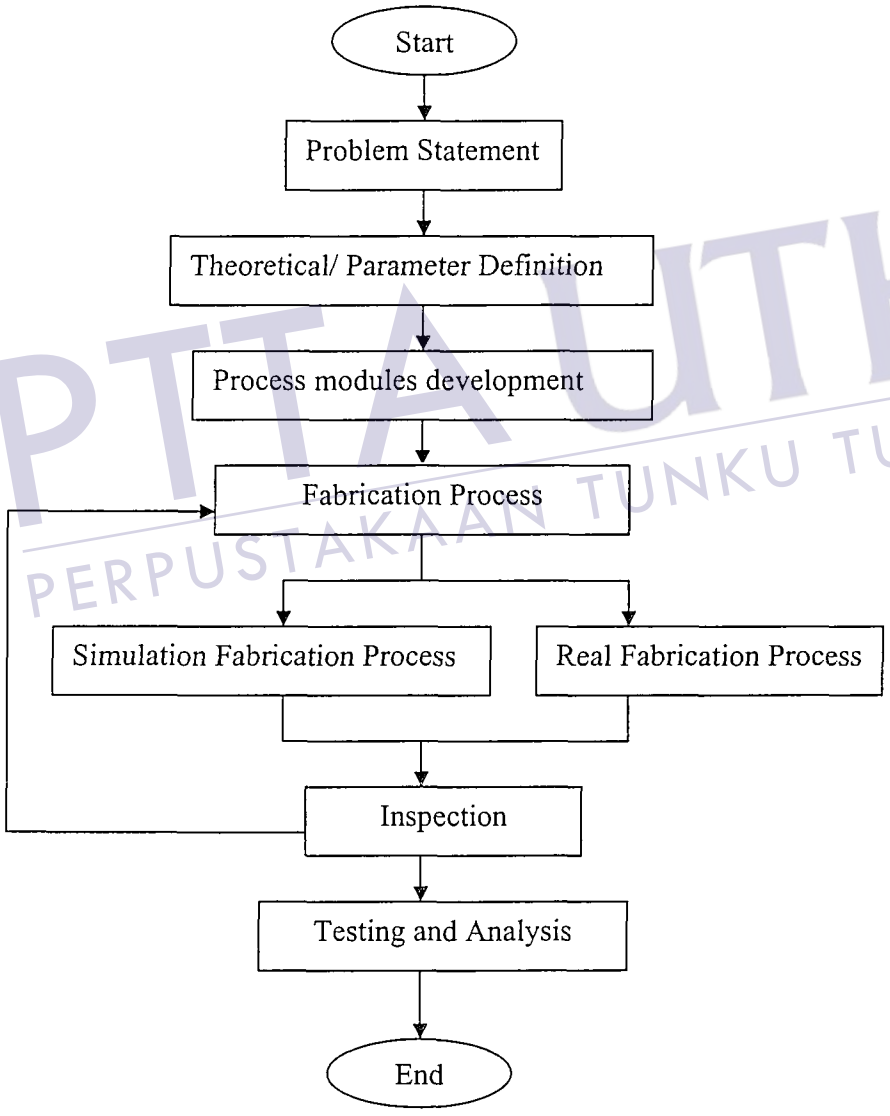

Figure1.1: The project flowchart

CHAPTER II

LITERATURE REVIEW

2.1 Introduction

This chapter will highlight on the understanding of transistor device mainly MOSFET (Metal Oxide Semiconductor Field Effect Transistor). This project focuses on the fabrication process of MOSFET devices. Prior to that, the characteristics and physical structure of PMOS transistor was studied.

2.2 The MOS Transistor

These devices are known as FET's (Field effect transistors), which consist of three regions; source, drain and gate. The resistance path between the drain and source is controlled by applying a voltage to the gate. This varies the depletion layer under the gate and thus reduces or increases the conductance path. The FET input impedance (unlike the BJT which is a few kΩ) is very high (~MΩ's) and as a result the gate current can be considered as zero.

2.3 P-Channel MOSFET (PMOS)

A transistor is considered as depletion type if both source and drain are connected by a channel. This channel is created by implantation ion or diffusion process. If there are no channel exists, the operation of transistor known as depletion operation. The depletion mode used mainly in analog circuit. A p-channel depletion mode transistor, which can conceptually possible, has never been used in practical circuits.

In this project, the enhancement PMOS transistor will be used. It is relatively easy to make as an enhancement mode device, which is preferred choice for digital application since it minimizes the standard power dissipation.

2.3.1 Structure of P-Channel MOS (PMOS) Transistor

The transistor is formed on an n-type silicon body or substrate. Typical doping concentrations for the body are 10^{14} to 10^{18} cm^{-3}. The dopant concentrations will be assumed uniform throughout the body. For p-channel MOS, typically the dopant material is Boron (Thomas,2000)[4]. The center part of the structure is covered by an insulator (typically silicon dioxide, which often referred to simply as oxide). The body interface to the oxide is often called the surface.

A low resistivity electrode, called the gate, is formed on the top oxide. Contemporary processes commonly use polycrystalline silicon (polysilicon) for the gate.

In this case, metal was used instead of polysilicon. The two regions shown on the sides are formed by implanting or diffusing acceptor atoms, with the gate acting as a mask against the implant/diffused region. This mask receives the acceptor atoms itself and prevents them from landing under it (Douglas and Eshraghian,1988)[1].

The region between the source and drain is called 'channel'. The channel width (W) and length (L) of individual transistors can vary greatly (from a fraction of micrometer to several hundred micrometer), depending on the circuit needs. In digital circuits, L is normally kept as the minimum value possible (Zant,2000)[12]. The internal structure of p-channel MOS transistor depicts in figure 2.1.

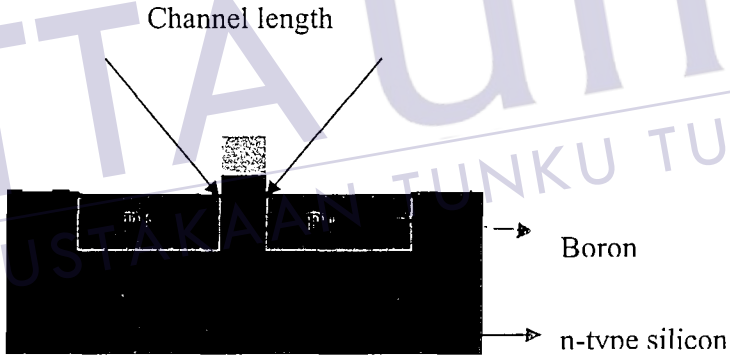

Figure 2.1: An internal structure of p-channel MOS transistor

2.4 Qualitatitive I-V Behavior of PMOS Transistor

MOS transistor with p-type channel (PMOS) transistor easily be fabricated. In fact, the first commercial MOS transistor and integrated circuits used PMOS devices

because it was easier to control fabrication process of PMOS technology (Jaeger,1997) [14]. The enhancement mode PMOS device is fabricated by forming p-type source and drain regions in an n-type substrate as depicted in the device cross section in figure 2.2. By refering to the figure, the source, drain and body of the PMOSFET are all grounded.

In the figure2.2, the condition shown are those for an unbiased device; however, the application of negative voltage of suitable magnitude ($0>V_{TH}$) between gate and source will give rise to the formation of a channel (p-type) between the source and drain and current may then flow if the drain is made negative with respect to the source. In this case the current is carried by holes as opposed to electrons (as in the case for nmos device). In consequence, PMOS transistors are inherently slower than NMOS, since hole mobility μ_p is less by a factor of 2.5 apporoximately than electron mobility μ_n.

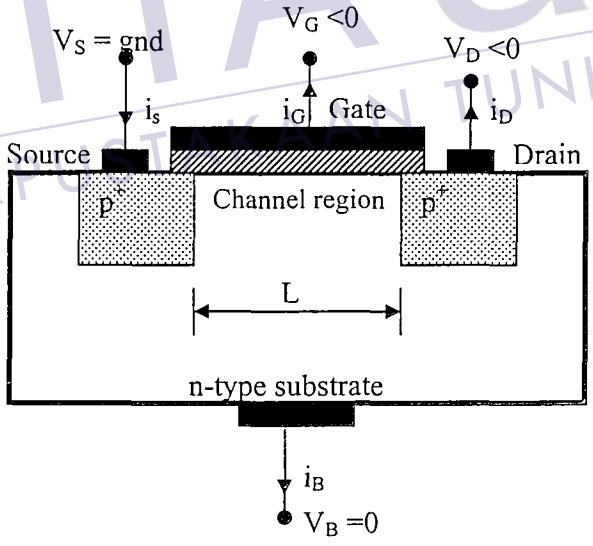

Figure 2.2: Cross section of an enhancement-mode PMOS transistor

2.5 Characteristics of the PMOS Transistor

Three sets of condition (cutoff region, linear region and saturating region) of enhance-mode PMOS transistor show as figure 2.3(a) through 2.3(d). In order to establish the channel in the first place a minimum voltage level of threshold voltage, V_{TH} must be established between gate and source and between gate and substrate. Figure 2.3(a) indicates the conditions prevailing with the channel established but no current flowing between source and drain ($V_{SD} = 0$). The condition prevailing when current flows in the channel by applying a voltage V_{DS} between drain and source. It corresponding i_{SD} drop = V_{SD} along the channel.

This result in the voltage between gate and channel varying with distance along the channel with the voltage between gate and channel being a maximum og V_{SG} at the source end. Since the effective gate voltage is $V_G = V_{SG} - V_{TH}$ (no current flows when $V_{SG} \leq -V_{TH}$) there will be voltage available to invert the channel at the drain. The limiting condition comes when $V_{SD} = V_{SG} - V_{TH}$. For all voltages $V_{SG} + V_{TH} \geq V_{SD} \geq 0$, the device is in the nonsaturated regoin of operation which is condition in figure 2.3(b).

When V_{SD} is increased to a level greather than $V_{SG} - V_{TH}$, in this case, an $i_{SD}=V_{SG}-V_{TH}$ takes place over less than the whole length of the channel so that over part of the channel, near the drain, there is no electric field available to give rise to an inversion layer to create the channel. The channel is, therefore 'pinched off' as indicated in figure2.3(c). Diffusion current completes the parh from source to drain in this case, causing the channel to exhibit a high resistance and behave as a constant current source. This region, known as saturation, is characterized by almost constant current for increase for $V_{SD} \geq (V_{SG} + V_{TH}) \geq 0$.

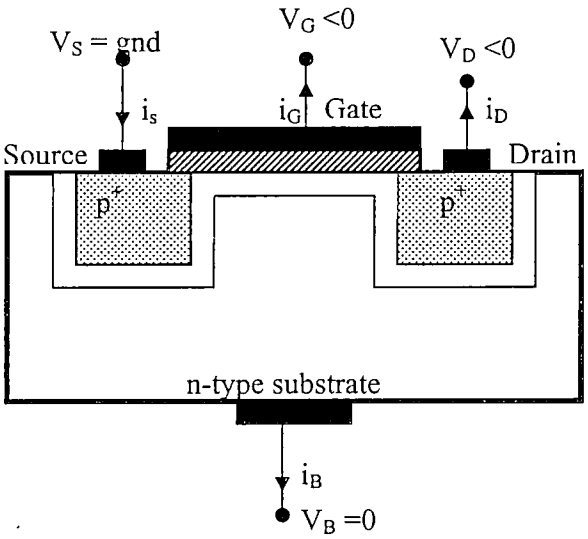

Figure 2.3(a) : $V_{SG} \leq V_{TH}$ – cut off region

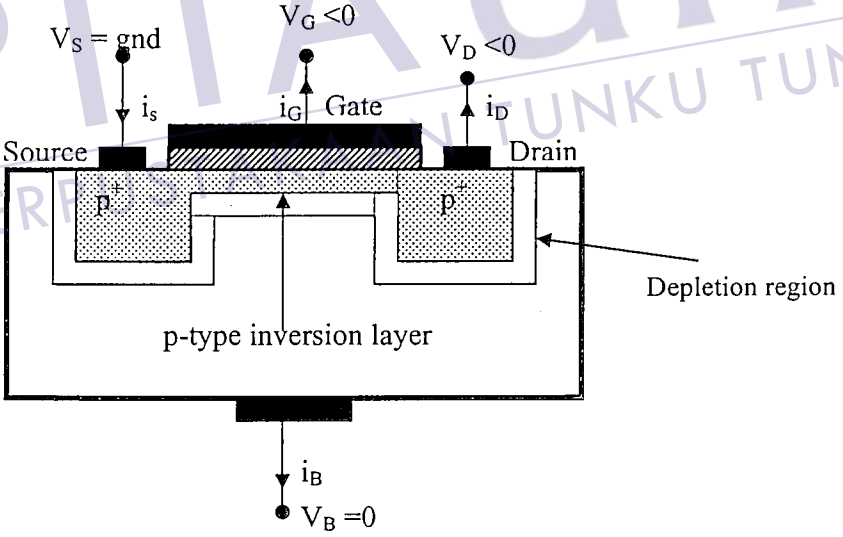

Figure 2.3(b): $V_{SG} \geq V_{TH}$ – linear region

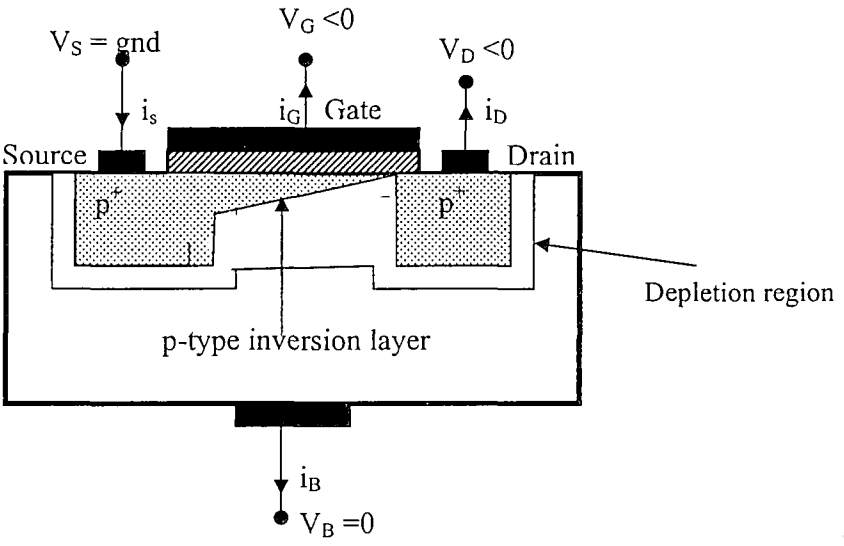

Figure 2.3(c): PMOS with channel just pinch off at the drain

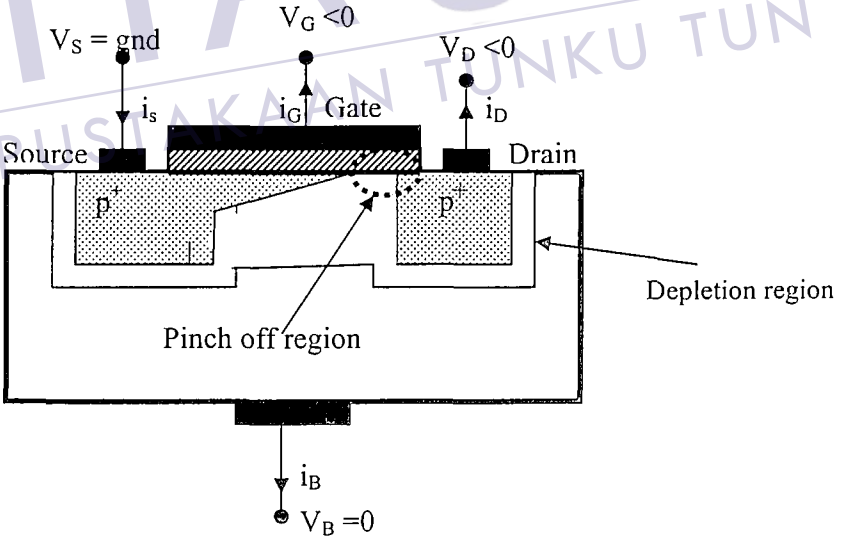

Figure 2.3(d) : Pinch off for $V_{SD} \geq (V_{SG} + V_{TH}) \geq 0$

The mathematical model for the PMOS transistor is summarized in equation 2.1 through 2.3 for all region.

$K_p = \mu_p C''_{ox} (W/L)$ $i_G = 0$ and $i_B = 0$

Cutoff region : $i_{SD} = 0$ for $V_{SG} \leq -V_{TH}$ (2.1)

Linear region : $i_{SD} = K_p (V_{SG} + V_{TH} - (V_{SD}/2) V_{SD}$ for $V_{SG} + V_{TH} \geq V_{SD} \geq 0$ (2.2)

Saturation region : $(V_{SG} + V_{TH})^2 (1 + \lambda V_{SD})$ for $V_{SD} \geq (V_{SG} + V_{TH}) \geq 0$ (2.3)

Where,

K_p = transconductance parameters

C''_{ox} = oxide capacitance per unit area (F/cm^2)

W = channel width which is measured perpendicular to the direction of current

L = channel length which is measured in the direction of current in the channel

λ = channel-length modulation parameter

μ_p = Hole mobility

V_{SG} = source-gate voltage ; V_{SD} = source-drain voltage; V_{TH} = theshold voltage

2.6 Relationship between Gate Length, Threshold Voltage and Gate Oxide Thickness

The length and width of a tarnsistor are the two most important dimensions of a transistor (Sami,(2004)[8]. When the people talk about the gate size of spesific technology, they are reffering to the minimum gate length. The critical dimensions that needs to be engineered are gate length(L_G), the gate oxide thickness ($t_{ox)}$, the depletion depths under the gate, the source-drain junction depth (x_j) and steepness of the source-drain junction. All these quantities must be scaled together. In this project, the different of length gate (L_G) and oxide thickness are take into consideration to determine the threshold voltage and performance of PMOS transistor.

2.6.1 Gate Length

Interm of layout design, the length of the transistoris the distance between the source and the drain of a transistor. This may not be intuitive, because the physical dimension of the transistor length is smaller than the width. In term of transistor performance, the length of the transistor is the distancesurable current flow. The gate voltage that controls the flow of current. If the distance between the source and drain is reduced, the gate voltage has a stronger influence in enabling current flow. More current conceptually means faster performance. Refer to the equation 1.1 (Chapter I)

$$\tau_D \approx \frac{C_L V_D}{I_D} \infty \frac{C_L L_G t_{ox} V_D}{(V_D - V_{TH})^2}$$

it showed that the time delay τ_D, proportional to the length gate,L_G and threshold voltage,V_{TH}. From the time delay, it can be determine the performance of the transistor.

The length of a transistor in terms of manufacturing capabilities is the narrowest possible piece of polysilicon (poly) that can be manufactured reliably. Smaller poly dimension and thus smaller transistor result in smaller ICs, so it is attractive to use the minimum gate length to minimize chip area [14]. However, these largely experimental techniques have never been proven in a manufacturing environment. The development of a reliable, manufacturable cost-effective lithography technique is absolutely essential to continued progress in CMOS technology.

2.6.2 Gate Oxide Thickness

The electrical thickness of gate insulator must decrease with the channel length. Recently, studies of tunnelling through thickness oxide have shown that silicon dioxide can potentially be thinned to slightly below 2 nm before the leakage current and the associated dissipation become so large as to be unacceptable (Tsividis,1999)[17]. For equivalent electrical SiO_2 thickness below 2 nm, thicker gate insulators with a higher dielectric constant than silicon dioxide are being considerate to reduce the tunnelling current through the gate insulator.

2.6.3 Threshold Voltage

The gate structure of a MOS transistor consists, electrically, of charges store in the dielectric layers and in the surface interfaces as well as in the substrate itself. Switching an enhancement mode MOS transistor from the off to the on state consists of applying sufficient gate voltage to neutralize these charge and enable the underlying silicon to undergo an inversion due to the electric field from the gate. Increasing voltage source, V_{SB} causes the channel to be depleted of charge carriers and thus, the threshold voltage is raised. For the enhancement-mode PMOS transistor, threshold voltage, $V_{TH} < 0$.

2.7 Fabrication Process

The production of semiconductor is a challenging technological process. The success of operation management and production control technique is critically dependent upon the availability and performance of highly sophisticated and very expensive process equipment. Manufacturing semiconductors, also called integrated circuits or chips, requires repetitive sequences of similar processing operations such as oxidation, etch, photolithography, diffusion, ion implant and metallization.

2.7.1 Cleanroom Cleanliness

The fabrication area consisted of a large room with the work station (called hoods) arranged in rows so that the wafers could move sequentially through the process, never being exposed to dirty air. Normal air is so laden with contaminants that it must be treated before entering a cleanroom. Air cleanliness levels in cleanrooms are identified by the particulate diameters and their density in the air. Air quality is designated by the *class number* of the air in the area as defined in Federal Standard209E (Ruska,1987)[18]. This standard designates air quality in the two categories of particle size and density. The class number of an area is defined as the number of particles 0.5μm or larger in a cubic foot of air. Advancing chip sensitivity has identified smaller and smaller tolerable particle sizes for each generation of chip feature size.

Federal Standard 209E defines class number at 0.5μm particle size, successful wafer fabrication processing requires tighter controls. With class number of 1000 contains maximum 0.5μm particles per cubic foot. In this project the work station fabrication process had been done in class 1000 room and photolithography process in class 100 yellow room (fig 2.4). The measurement of cleanliness of each room had been done and the result had been shown in table 2.1.

.

Figure 2.4 : Class 100 yellow room for photolithography process

Table 2.1 : Cleanroom cleanliness measurement

White Room – Class 1000	**Yellow Room – Class 100**
Area 1 – 54cm3 Area 2 – 111cm3 Area 3 – 38cm3 Area 4 – 64cm3 Total Particle – 267cm^3	Area 1 – 17cm3 Area 2 – 19cm3 Area 3 – 15cm3 Total Particle – 51cm3

2.7.2 Cleaning Process

To achieve high production yield and device reliability, it is essential to eliminate all sources of contamination. Surface cleaning is particularly important prior to high temperature process because impurities react and diffuse at much higher rates at elevated temperature. There are two types of cleaning process which are wet cleaning and dry cleaning. In this project the wet cleaning will be used. Chemical cleaning is standard for the wafer clean, using solvent asid such as Buffered Oxide Etching (BOE) to remove organic and inorganic contaminants residue, respectively. It is usually followed by deionized (DI) water rinse and spin dry process.

Most common process used is the RCA wet cleaning process. RCA cleaning process is the composition of NH_4OH-H_2O_2-H_20 (1:1:5 – 1:1:7 at 70°C to 80°C). This composition can effectively remove organic contamination and particle by oxidation. It also can be used for complete fulfillment of an ultra clean wafer surface; it should be free from particle, organic contamination, metal contamination, surface microroughness & native oxide. Figure 2.5(a) and 2.5(b) shows clean process equipment.

The RCA formulas have been proven durable over the years, and are still the base cleaning process for most pre-furnace cleaning. Improvements in chemical purity have kept pace with industry cleaning needs. These solutions have been found to be as effective as the more concentrated versions. Additionally, they produce less micro roughing and are cost effective and easier to remove.

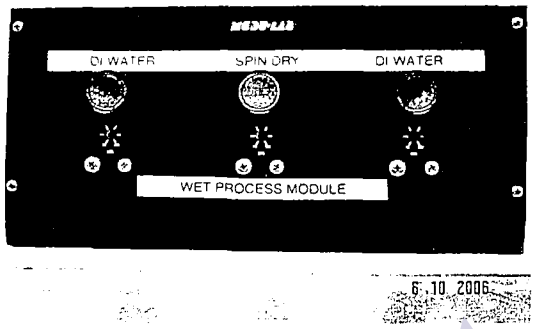

Figure 2.5(a) : Cleaning Process Section

Figure 2.5(b) D.I water

2.7.3 Oxidation Process

Oxidation is one of the most important thermal processes. It is an adding process, which adds oxygen to a silicon wafer to form silicon dioxide to a silicon surface [8]. The oxidation rate controlled by four conditions:

i. Temperature
ii. Pressure
iii. Time
iv. Crystal orientation

The oxidation process can be carried out through wet or dry conditions in this project. The process will be done by furnace with horizontal reactor. Dry oxidation simply flow oxygen gas over the silicon and reaction that occurs is:

$$Si + O_2 \longrightarrow SiO_2 \qquad (2.5)$$

Wet condition produced the fastest reaction rate. Wet condition can be developed by flowing oxygen through wafer so the oxygen carries it with water vapor. The reaction that occurs is:

$$Si + 2H_2O \longrightarrow SiO_2 + 2H_2 \qquad (2.6)$$

2.7.3.1 Horizontal Tube Furnace

Horizontal tube furnaces have been used in the industry since the early 1960s for oxidation, diffusion, heat treating and various deposition processes. They were first developed for diffusion processes in germanium technology and to this day are often call diffusion furnaces or tube furnace. Horizontal designs evolved into vertical designs with a number of advantages.

Basic single horizontal three-zone tube furnace is shown in fig 2.6. It consists of a long ceramics tube, with coils of copper tubing on the inside furnace. Each of the coiled tubes defines a zone and is connected to separate power supply operated by a proportional band controller. Furnace may have up to seven separate zones. Inside the furnace tube is quartz reaction tube that serves as the reaction chamber for the oxidation or other processes. The reaction tube may itself be inside a ceramic liner called a muffle. The muffle acts as a heat sink fostering a more even heat distribution along the quartz tube.

Thermocouples are positioned against the quartz tube and send temperature information to the proportional band controllers. The controllers proportion power to the coils, which in turn heat the reaction tube by radiation and conduction. Radiation heating comes from the energy given off by the coil and impinging on the tube. Conduction takes place where the coils touch the tube. These controllers are very sophisticated and can control temperatures in the center zone to plus or minus 0.5°.

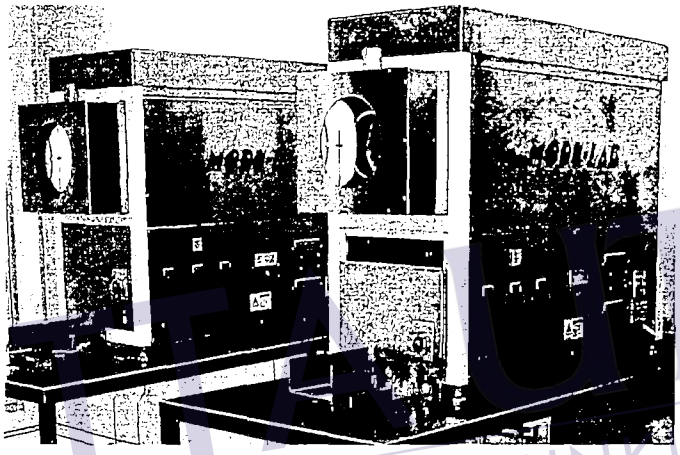

Figure 2.6: Furnace Equipment

2.7.3.2 Dry Oxygen

When oxygen is used as the oxidant, it is supplied from the facility source or from tanks of compressed oxygen located in the source cabinet. It is imperative that the gas be dry; that is, not contaminated with water vapor. The presence of water vapor in the oxygen would increase the oxidation rate and cause the oxide layer to be out of specification. Dry oxygen oxidation is the preferred method for growing the very thin (<1000 angstroms, Å) gate oxides required for MOS devices.

2.7.3.3 Water Vapor Source

There are several methods used to supply water vapor (steam) into the oxidation tube. In this project Bubbler water vapor source is used to growth oxide layer onto silicon wafer during steam or wet oxidation process. For oxidation, the bubbler liquid is deionized (D.I. water) (Fig 2.7) heated close to the boiling point (98 to 99°C), which creates a water vapor in the space above the liquid. As the carrier gas is bubbled through the water and passes through the vapor, it becomes saturated with water. Under the influence of the elevated temperature inside the tube, the water vapor becomes steam and causes the oxidation of the silicon surface. With bubblers technique, there is always concern about contamination potential is heightened by the need to open the system periodically to replenish the water.

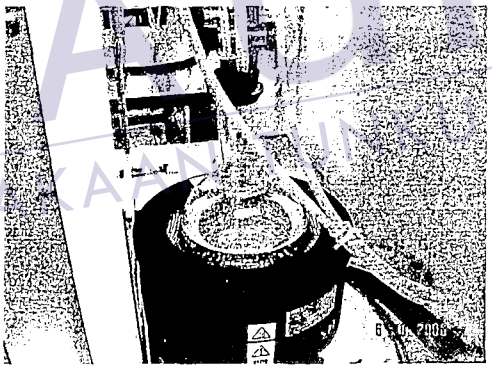

Figure 2.7 : Bubler water vapor source

2.7.4 Diffusion

Diffusion has historically been the most important processing steps used in the fabrication of monolithic integrated circuits. For many years, diffusion was the primary method of introducing impurities such as Boron, Phosphorous, and antimony into silicon to control majority-carries type and resistivity of layer formed in the wafer. Because of the most commonly used tool for silicon doping was the high-temperature quartz tube furnace, it has been called the 'diffusion furnace' ever since in figure 2.6.

The commonly used diffusion doping process sequence is predeposition, then drive-in. At a first layer of dopant oxide, B_2O_3 is deposited on the wafer surface at high temperature, followed by thermal oxidation process that consumes the residue dopant gas and grows the layer of silicon dioxide, which caps the dopant and prevent out-diffusion.

A deposition depends on the presence of a concentration of dopant atom vapor in the tube. The vapors are created from a dopant source located in the source cabinet of the tube furnace and pass into the tube with a carrier gas. The chemical reaction for the predeposition and cap oxidation (drive in) for the most commonly used Boron source can be expressed by [4].

Boron: Predeposition : $B_2H_6 + 2O_2 \longrightarrow B_2O_3 + 3H_2O$ (2.7)

Drive-in : $2B_2O_3 + 3Si \longrightarrow 4B + 3SiO_2$ (2.8)

2.7.5 Photolithography

Photolitogrphy is the core of the ICs manufacturing process. Photolithography is the patterning process that transfers the design pattern from the mask or reticle to the photoresist on the wafer surface. Photolithography was first used in the printing industry and has long been used to make printed circuit board. It was adapted in semiconductor industry for transistor and integrated circuit in the 1950s.

Photolithography is one of the most critical operations in semiconductor processing. It is the process that sets the surface dimensions on the various parts of the device and circuits. The goal of the operation is twofold. First, is to create in and on the wafer surface pattern whose dimensions are as close to the design requirement as possible. This goal is referred to as the resolution of the images on the wafer. The pattern dimensions are referred to as the feature sizes or image size of the circuit.

The second goal is the correct placement (called alignment or registration) of the circuit pattern on the wafer. The entire circuit pattern must be correctly placed on the wafer surface and the individual parts of the circuit must be in the correct position relative to each other. In a circuit, the effects of misalignment mask layers can cause the entire circuit to fail.

The photolithography process includes three major steps; photoresist coating, alignment and exposure and photoresist developing. To achieve high resolution, photolithography also has soft bake and chilling process. After developing process, the wafer through patterned inspection process and if a wafer failed to pass the inspection, it by passed the hard bake steps, the photoresist stripped, and whole process repeated until it passed the inspection (Jacob and Harry,1998)[13],(fig 2.8(a) and 2.8(b)). The selection

of a resist and development of resist process is a detail and lengthy procedure. Once a resist process is established, it is changed very reluctantly. In this project, photolithography process had been done in a room class 100 and named as yellow room.

Figure 2.8(a): Spin on-dopant Equipment

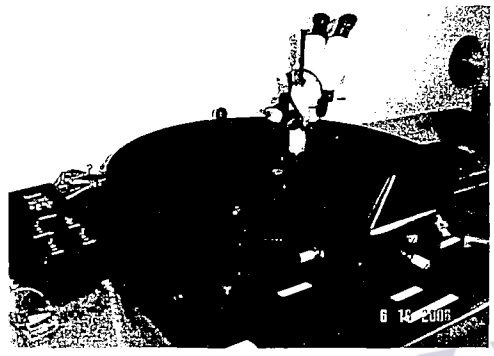

Figure 2.8(b) : Transfer Patern Equipment

2.7.6 Metallization

A variety of conductors is applied in IC chip manufacturing. Metals with high conductivity are widely used for interconnections forming microelectronics circuits. Metallization is an adding process that deposits metal layers on the wafer surface. Metal such as copper and aluminum are good conductors, widely used to make conducting lines to transport electrical power signals. In this project, the metal used was aluminum and the process will be done by PVD equipment.

Sputter deposition (sputtering) is a process adapted to semiconductor needs. Sputtering is a process that can deposit any material on any substrate. It is widely used

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