A STUDY OF VARIABLE I-REGION THICKNESS EFFECTS ON PIN DIODE SWITCHING SPEED

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The PIN diodes are widely used in RF, UHF and microwave circuits as it acts as a current controlled resistor at these frequencies. PIN diode performance is greatly influenced by the geometrical size of the device, especially in the intrinsic region. The change in geometry in the intrinsic will result the differences the most important parameters value of the PIN diode including the carrier lifetime and transit time frequency. In this research, the switching speed performance of PIN diode with different I-region layer thickness, \( W \), is analyzed to study their correlation. A PIN diode structure has been designed in the Sentaurus Technology Computer Aided Design (TCAD) tools. The I-layer thickness (or width) is varied from 5\( \mu \)m to 100\( \mu \)m to investigate its effects on the current-voltage (\( I-V \)) characteristics and a few other important parameters have been extracted. These parameters are used to analyze the switching speed performance of the Silicon (Si) PIN diode. The study is validated by theory calculation as well as experimental work using practical diode with driver circuit.
CHAPTER I

INTRODUCTION

PIN diode's name is attributed by its overall structure where P is representing P type layer, I is representing intrinsic layer and N is representing N type layer as shown in Fig. 1. The existence of intrinsic region makes it ideal for attenuator, fast switches and photo detectors. Hence, PIN diodes are used extensively in the microwave and RF application due to its ability to control the magnitude and phase of the signals [1,2]. Its exploitation as the switching element in the microwave and RF circuits is based on the difference of the characteristics of PIN diode at the forward and reverse bias condition [3].

Figure 1. PIN Diode Structure
When the PIN diode is forward biased, holes and electrons are injected into the I-region (or referred as layer). This charge consists of holes and electrons which have a finite lifetime before recombination. Although carrier lifetime, $\tau$, indeed a factor of PIN diode operations, the thickness of the I-layer, $W$, is equally important which relates to the transit time frequency of the PIN diode. By varying the I-layer width and diode area it’s possible to construct PIN diode of different geometrics to result in the same shunt resistance, $R_s$ and total capacitance, $C_T$ characteristic. These devices may have similar small signal characteristics.

However, a thicker I-region diode would have a higher bulk or RF breakdown voltage and better distortion properties. On the other hand, the thinner device would have faster switching speed. As a result, this project is embarked to study the effect of variable thickness I-region layer, $W$, towards the switching speed performance of PIN diode. By optimizing and characterizing the process modules and parameter using Sentaurus TCAD tools, the recipe for in-house fabrication process is developed. Finally, the effect of different I-region layer thickness on PIN diode switching speed model is analyzed.

1.1 Background Study

A PIN diode is a semiconductor device that operates as a variable resistor at RF and microwave frequencies. The resistance value of the PIN diode is determined only by the forward biased dc current. It is a silicon semiconductor diode in which a high resistivity intrinsic I-region is sandwiched between a P type and N type region. In general, the chip wafers almost intrinsically pure silicon. P-region is then diffused into one diode surface and an N-region is diffused into the other surface. The resulting intrinsic or I-region thickness, $W$ is a function of the thickness of the original silicon wafer.

The performance of the PIN diode primarily depends on chip geometry and the nature of the semiconductor material in the finished diode, particularly in the I-region. The PIN diode characteristics are controlled thickness I-regions having long carrier lifetimes and high resistivity [1]. On the other hand, the thinner device would
have faster switching speed. Using Sentaurus TCAD the thickness of the silicon PIN diode parameter performance is analyzed and discussed.

1.2 Objective

There are a few objectives to be achieved in this project:
(i) to determine the design architecture of silicon PIN diode
(ii) to simulate PIN diode structure using Sentaurus TCAD software
(iii) to simulate the PIN diode fabrication process and recipe using TCAD
(iv) to analyze the effect of different I-region layer thickness on PIN diode switching speed performance.

1.3 Scope of Study

Generally the scope of the project are:
(i) to analyze the output characteristic of the silicon PIN diode using Sentaurus TCAD software
(ii) make comparison of I-V performance of PIN diode when the value of $W$ is changed
(iii) obtain the I-V performance of PIN diode with variable I-region width, 6 μs, 11 μs, and 55 μs by using Sentaurus TCAD
(iv) simulation value is used to measure switching performance of each PIN diodes.
(v) a few experiment is setup to determine the switching performance of PIN diodes.
(vi) the suitable I-layer thickness will be varied in the range of 5 μm and 200 μm
(vii) the switching performance of PIN diode is determined and verified by using measurement, simulation and experimental method.
1.4 Problem Statement

There are several problems in order to complete this project. The range values of intrinsic thickness, \( W \), of Silicon PIN diode to get the better performance of this device. A thinner intrinsic layer is expected to produce higher current. The parameters of silicon PIN diode can be determined and it can be related with a calculation and make a comparison using Sentaurus TCAD. As such, in order to get thickness effect of the silicon PIN diode performance, this design must be simulated for several I-region thicknesses, \( W \). In this project, the switching performance of PIN diode will be investigated and analysed with different I-region width value to discover their relationship.

1.5 Expected result

(i) Through studies committed against variation of thickness in the PIN diode, current performance is directly proportional with a voltage

(ii) a fabrication process of Silicon PIN diode using Sentaurus TCAD software is developed

(iii) various thickness (W) effects on parameter performance are compared and analyzed

(iv) The switching speed performance of various I-layer thickness will be obtained

1.6 Chapter Summary

This chapter has introduced the problem statement, objectives, and scopes of study. Chapter 2 will further explain about the PIN diode structure and the device physics. The methodology to carry out the study is discussed in Chapter 3 while in Chapter 4, the results obtained are analysed. Finally, Chapter 5 summarize the report with the conclusion of the study as well as future recommendation.
CHAPTER 2

PROJECT BACKGROUND

2.1 PIN Diode Structure

The PIN diode receives its name from the fact that it has three main layers. Rather than just having a P type and an N type layer, the PIN diode has three layers such as shown in figure 2.1.

I. P-type layer
II. Intrinsic layer
III. N-type layer

![PIN Diode chip outline](image)

Figure 2.1. PIN Diode chip outline

The ability to control large RF signals while using much smaller level dc excitation makes the PIN diode suitable for applications including attenuating, modulating, limiting, phase shifting, and switching of RF and microwave frequencies signals. The performance of particular PIN diode in a given circuit or application is mainly determined by its design (geometry, semiconductor material used,
packaging), bias condition (forward or reverse bias level), and the frequency of the controlled signal.

The intrinsic layer of the PIN diode is the one that provides the change in properties when compared to a normal PN junction diode. The intrinsic region comprises of the undoped or virtually undoped semiconductor and in most PIN diodes it is very thin of the order of between 10 and 200 microns [7]. There are two main structures that can be used but the one which is referred to as a planar structure is shown in the figure 2.2 and the other is to use a mesa structure. The mesa structure has layers grown onto the substrate. PIN diodes are widely made of silicon, and this was the semiconductor material that was used exclusively until the 1980s when gallium arsenide (GaAs) started to be used.

![Figure 2.2. PIN diode with a planar construction](image)

Figure 2.3 is a schematic depiction of the cross-section of a PIN diode and the spatial distribution of the charge carrier concentration (without bias voltage). The critical factor for the radio frequency response is the (intrinsic) I layer between the highly doped P and N layers.

![Figure 2.3. Cross Section of PIN Diode without bias voltage](image)
The schematic depiction of the cross-section of a PIN diode and the distribution of the charge carrier concentration (without bias voltage) can be referred as the following:

1) p-conducting layer with higher charge carrier concentration
2) n-conducting layer with higher charge carrier concentration
3) Intrinsic layer of the width, \( W \) and cross sectional surface, \( A \)

2.2 PIN Diode Operation

Figure 2.4 shows the operating principles of a PIN diode. If forward bias is applied to the PIN diode, electrons and positive holes pour into the I-layer. The electrons and positive holes bond, generating those that become the forward current and those accumulate in the I-layer. Electrons and positive holes that accumulate in the I-layer function as carriers. The resistivity of the I-layer varies according to the quantity of electrons and positive holes, and these changes the high frequency series resistance [5].

![PIN Diode Operation Diagram](image)

Figure 2.4. PIN diode operation

Figure 2.5 shows the schematic of PIN diode. The advantages of this structure are a combination of good ohm contact and high energy collection efficiency. When particles penetrate the detector, electron-hole pairs are generated and current can be detected. Therefore, the energy of particles can be calculated from the current values [18].
2.2.1 N-type semiconductor

An N-type semiconductor (N for *Negative*) is obtained by carrying out a process of doping, that is, by adding an impurity of valence-five elements to a valence-four semiconductor in order to increase the number of free charge carriers (in this case negative). When the doping material from Group V such as phosphorus (P), arsenic (As), or antimony (Sb) is added, it gives away (donates) weakly-bound outer electrons to the semiconductor atoms. This type of doping agent is also known as *donor material* since it gives away some of its electrons.

2.2.2 P-type semiconductor

A P-type semiconductor (P for *Positive*) is obtained by carrying out a process of doping. When the doping material is added, it takes away (accepts) weakly-bound outer electrons from the semiconductor atoms. This type of doping agent is also known as *acceptor material* and the semiconductor atoms that have lost an electron are known as holes. The purpose of P-type doping using trivalent atom such as boron or aluminium is to create an abundance of holes.
2.2.3 Intrinsic semiconductor

An intrinsic semiconductor also called an undoped semiconductor or i-type semiconductor is a pure semiconductor without any significant dopant species present. The number of charge carriers is therefore determined by the properties of the material itself instead of the amount of impurities. In intrinsic semiconductors the number of excited electrons and the number of holes are equal: \( n = p \). The conductivity of intrinsic semiconductors can be due to crystal defects or to thermal excitation. In an intrinsic semiconductor the number of electrons in the conduction band is equal to the number of holes in the valence band [5].

2.3 PIN Diode Uses and Advantages

The PIN diode is suitably used in a number of areas as a result of its structure proving some properties which are of particular use. These are three of the main applications for PIN diodes, although they can also be used in some other areas as well.

2.3.1) High voltage rectifier: The PIN diode can be used as a high voltage rectifier. The intrinsic region provides a greater separation between the PN and N regions, allowing higher reverse voltages to be tolerated.

2.3.2) RF switch: The PIN diode makes an ideal RF switch. The intrinsic layer between the P and N regions increases the distance between them. This also decreases the capacitance between them, thereby increasing the level of isolation when the diode is reverse biased.

2.3.3) Photodetector: As the conversion of light into current takes place within the depletion region of a photodiode, increasing the depletion region by adding the intrinsic layer improves the performance by increasing the volume in which light conversion occurs.
The PIN diode is an ideal component to provide electronics switching in many areas of electronics. It is particularly useful for RF design applications and for providing the switching, or attenuating element in RF switches and RF attenuators. The PIN diode is able to provide much higher levels of reliability than RF relays that are often the only other alternative.

2.4 Parameter in PIN Diode

As shown in the table 2.3, silicon is the best choice in a pure intrinsic material because silicon is a very cheap compared with germanium in this project. Then silicon semiconductor consisting of a layer of intrinsic (high resistivity) material of finite thickness which is contained between highly doped P and N material. In general, silicon band gap is larger than germanium band gap, so very few electrons can jump into the gap. Therefore, current does not flow easily in it.

Table 2.3: Comparison between Chemical Properties of Silicon and Germanium [4]

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Silicon</th>
<th>Germanium</th>
</tr>
</thead>
<tbody>
<tr>
<td>Density</td>
<td>2.329 g cm⁻³</td>
<td>5.3234 g/cm³</td>
</tr>
<tr>
<td>Dielectric constant</td>
<td>11.7</td>
<td>16.2</td>
</tr>
<tr>
<td>Energy gap</td>
<td>1.12 eV</td>
<td>0.66 eV</td>
</tr>
<tr>
<td>Intrinsic resistivity</td>
<td>3.2·10⁵Ω cm</td>
<td>46 Ω cm</td>
</tr>
<tr>
<td>Conduction band effective density</td>
<td>2.78X10¹⁹ cm⁻³</td>
<td>1.04X10¹⁶ cm⁻³</td>
</tr>
<tr>
<td>Valence band effective density</td>
<td>9.84X10¹⁸ cm⁻³</td>
<td>6.0X10¹⁴ cm⁻³</td>
</tr>
<tr>
<td>Intrinsic carrier concentration</td>
<td>1.5X10¹⁰ cm⁻³</td>
<td>2.33X10¹⁰ cm⁻³</td>
</tr>
<tr>
<td>Breakdown field</td>
<td>3X10⁷V/cm</td>
<td>10⁷V cm⁻¹</td>
</tr>
<tr>
<td>Mobility electrons</td>
<td>1500 cm² V⁻¹ s⁻¹</td>
<td>3900 cm² V⁻¹ s⁻¹</td>
</tr>
<tr>
<td>Mobility holes</td>
<td>450 cm² V⁻¹ s⁻¹</td>
<td>1900 cm² V⁻¹ s⁻¹</td>
</tr>
<tr>
<td>Diffusion coefficient electrons</td>
<td>35 cm²/s</td>
<td>100 cm² s⁻¹</td>
</tr>
<tr>
<td>Diffusion coefficient holes</td>
<td>12 cm²/s</td>
<td>50 cm² s⁻¹</td>
</tr>
<tr>
<td>Electron thermal velocity</td>
<td>2.3X10⁵ m/s</td>
<td>3.1X10⁷ m s⁻¹</td>
</tr>
<tr>
<td>Hole thermal velocity</td>
<td>1.65X10⁵ m/s</td>
<td>1.9X10⁷ m s⁻¹</td>
</tr>
</tbody>
</table>
2.4 Related Theories and Calculation

The followings are the calculation formulas used to find the width, $W$ of the depletion region (Semiconductor devices: basic principles / Jasprit Singh 2001).

To find the minority charge density:

$$n_p = \frac{n_i}{N_a} \text{ and } p_n = \frac{n_i^2}{N_a} \tag{1}$$

The electron diffusion length

$$L_n = \sqrt{D_n \tau_n} \text{ and } L_p = \sqrt{D_p \tau_p} \tag{2}$$

Built in Voltage

$$V_{bi} = \frac{kBT}{e} \ln \left( \frac{N_a N_d}{n_i^2} \right) \tag{3}$$

To find the depletion width

$$W = \left\{ \frac{2E}{e} \left( \frac{N_a + N_d}{N_a N_d} \right) \left( V_{bi} + V_a + V_i \right) \right\}^{\frac{1}{2}} + x_i \tag{4}$$

To find the generation- recombination current

$$I_{GR} = \frac{eA W n_i}{2\tau} \tag{5}$$

To find the prefactors to the recombination – generation current is

$$I_0 = eA \left( \frac{D_p P_n}{L_p} + \frac{D_n n_p}{L_n} \right) \tag{6}$$

To find the current

$$I = I_0 \left( \exp \left( \frac{eV}{kBT} \right) \right) + I_{GR} \left( \exp \left( \frac{eV}{2kBT} \right) \right) \tag{7}$$
2.3.1 Forward Biased of PIN Diodes

When a PIN diode is forward biased, holes and electrons are injected from the P and N regions into the I-region. These charges do not recombine immediately. Instead, a finite quantity of charge always remains stored and results in a lowering of the resistivity of the I-region. The quantity of stored charge, $Q$, depends on the recombination time, $\tau$, and the forward bias current, $I_F$, as shown in Equation (8).

$$Q = \tau I_F$$  \hspace{1cm} (8)

The resistance of the I-region under forward bias, $R_S$, is inversely proportional to $Q$ and may be expressed as (9):

$$R_S = \frac{W^2}{(\mu_N + \mu_P)Q}$$  \hspace{1cm} (9)

where:  
$W$ = I-region width  
$\mu_N$ = electron mobility  
$\mu_P$ = hole mobility

This equation is independent of area. In the real world the $R_S$ is slightly dependent upon area because the effective lifetime varies with area and thickness due to edge recombination effects. The above equation is valid for frequencies higher than the transit time of the I-region, where

$$f > \frac{1300}{W^2}$$  \hspace{1cm} (10)
2.3.2 Reverse Biased of PIN Diodes

At high RF frequencies when a PIN diode is at zero or reverse bias, it appears as a parallel plate capacitor, essentially independent of reverse voltage,

\[ C = \frac{\varepsilon A}{W} \]  \hspace{1cm} (11)

where: \( \varepsilon \) = silicon dielectric constant
\( A \) = junction area

This equation is valid for frequencies above the dielectric relaxation frequency of the I-region:

\[ f = \frac{1}{2\pi \rho \varepsilon} \]  \hspace{1cm} (12)

where: \( \rho \) = Resistivity of Silicon

2.3.3 Equivalent Circuits

Figure 2.6 represents the equivalent circuit for forward and reverse biased.

![Equivalent Circuits](image)

(a)  \hspace{4cm} (b)

Figure 2.6. The Corresponding Equivalent Circuits; (a) forward bias and (b) reverse bias.
2.4 Switching Speed Characteristic

A commonly used definition for the switching speed of a PIN Diode is the time required to change the level of stored charge in its intrinsic region. In most applications (switching, phase shifting, etc), the switching speed would be the time required to either store or deplete the charge in the diode's intrinsic region. This time depends on the diode physical parameters as well as the drive circuits used and bias points at which the diode is being operated [9]. There are many ways that can be applied to find the switching performance of PIN diode. Basically it can be referred as the turn-on and turn-off time.

2.4.1 Turn-off time: Forward to Reverse Bias

![Figure 2.7. Turn-off time](image)

Figure 2.7 illustrates the turn-off time of a PIN diode. When a PIN diode is forward biased by current, $I_F$, the current flow results in charge, being stored in the I-region. This stored charge condition causes the PIN diode to be in the low resistance state. If the forward bias current is suddenly removed, the positive and negative charges in the PIN diode will recombine in a time period called $\tau$, the minority carrier lifetime. If a large reverse voltage is applied the forward conducting PIN diode, a reverse current, $I_R$, flows. $T_{off}$, or the forward-to-reverse switching time, is expressed in terms of $I_F$, $I_R$, and lifetime $\tau$, as in (13),

$$T_{off} = \tau \ln \left( 1 + \frac{I_F}{I_R} \right)$$

(13)
The elapsed time between the zero crossing of the reverse current \( (t_0) \) and the moment where the reverse current reaches ninety percent down from its maximum value \( (t_2) \) are called the reverse recovery time \( (t_{rr}) \) or turn-off time \( (T_{off}) \). These reverse recovery time commonly used in industry as a figure of the switching capability of a PIN diode.

The first state \( (t_0 \text{ to } t_1) \) is a plateau of constant reverse current and impedance and is called the delay time. This time is proportional to the ratio of forward current \( I_F \) and peak current \( I_R \), thus a reduction of the turn-off time can be achieved by decreasing this ratio and changing the delay time.

The second state \( (t_1 \text{ to } t_2) \) is known as the transition time. During this period, the impedances of the diode increases rapidly while the magnitude of the reverse current decreases. This transition time depends primarily on diode design (geometry and materials), and only slightly on the forward bias current. The transition time determines the minimum realizable turn-off time for a given device.

### 2.4.2 Turn-on time: Reverse to forward Bias

![Figure 2.8. Turn-on Time](image)

When forward bias is first applied, holes and electrons are injected from the P and N layers into the intrinsic layer. During the first part of the transition the diode impedance remains high until holes and electrons meet at the middle of the intrinsic layer. Once the carrier meet, the depletion region has been eliminated, charge starts to be stored in the intrinsic region decreasing the diode's impedance. The charge stored increases until it reaches its steady state value that is given by equation (8).
The speed at which the charge is injected and stored, and thus the turn-on time of the diode, depends on the intrinsic region geometry, and composition, as well as the magnitude and rate of a given diode is therefore limited by the circuit topology, parasitic impedances (especially inductive elements) and driver characteristics.

For most PIN diodes, the turn-on time is usually shorter than the turn-off time and is not considered the important parameter in the determining the switching speed of a PIN diode.
2.5 Fabrication Process of PIN Diode

The fabrication process of PIN diode involve many steps. These steps were varied depend on the specification including diode applications. Since the process are quite similar to each, hence the following fabrication steps are considered as the reference.

2.5.1 Fabrication and characteristics of thick PIN detector
References: http://www.paper.edu.cn

(a) oxidation
(b) photolithography for main junction and protect ring
(c) P⁺ implantation
(d) photolithography for thin silicon dioxide
(e) N⁺ implantation
(f) aluminum spottering

Figure 2.9. Schematic process flow for the fabrication of a 1mm PIN diode N-type.
2.5.2 Fabrication of a Silicon PIN Diode for Radiation Detection [9]

This paper explained in detail the process involve in fabrication of Si PIN diode which mainly designed for radiation detection. It uses lithography process which involve masking and deposition of material.

Figure 2.10. Schematics of the Fabrication Process Integration
2.5.3 Fabrication Process of Silicon Carbide PIN Diode [10]

Table 2.4 shows the Silicon Carbide (SiC) PIN diode processing outline. The paper discussed and explained in detail about the steps involved in the fabrication process. However, this process is meant for SiC PIN diode. Hence, the solution has to be slightly different since the study is carried out for silicon PIN diode. On the other hand, a summary of device parameter used in the simulations and fabrication process are also listed in Table 2.5.

Table 2.4: SiC PIN Diode Processing Outline

<table>
<thead>
<tr>
<th>No</th>
<th>Process / Steps</th>
<th>Layer</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td><strong>Receive Sample</strong>&lt;br&gt;Size: 3” wafer&lt;br&gt;Doping: n-type&lt;br&gt;Polytype: 4H-SiC&lt;br&gt;Orientation: 8.02°&lt;br&gt;Resistivity: 0.020&lt;br&gt;Thickness: 395.0μm</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>Dice sample&lt;br&gt;Pieces: 6 of equal area&lt;br&gt;Cut: One parallel to major flat, Two parallel to minor flat.</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>Clean sample&lt;br&gt;<em>Method</em>: Solvent and Piranha</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>Grow intrinsic layer&lt;br&gt;<em>Method</em>: CVD with Epigress&lt;br&gt;<em>Thickness</em>: 6μm</td>
<td>i-layer</td>
</tr>
<tr>
<td>5</td>
<td>Grow p-type layer&lt;br&gt;<em>Method</em>: CVD with Epigress&lt;br&gt;<em>Thickness</em>: 1.1μm</td>
<td>p-layer</td>
</tr>
<tr>
<td>6</td>
<td>Deposit SiO₂ mask&lt;br&gt;<em>Method</em>: LPCVD with Tempress&lt;br&gt;<em>Thickness</em>: 500Å</td>
<td>SiO₂</td>
</tr>
<tr>
<td>7</td>
<td>Deposit metal mask&lt;br&gt;<em>Method</em>: E-Beam Evaporation&lt;br&gt;<em>Layer 1</em>: 100Å of Ti&lt;br&gt;<em>Layer 2</em>: 5000Å of Au</td>
<td>Au Ti</td>
</tr>
<tr>
<td>8</td>
<td>Photolithography of mesa mask&lt;br&gt;<em>Photoresist</em>: Positive (AZ-1518)&lt;br&gt;<em>Develop</em>: 5:1 (Water : AZ 351 Developer) or 1:1 (Water : AZ Developer)</td>
<td>Photomask</td>
</tr>
<tr>
<td>9</td>
<td>Wet etch mesa mask&lt;br&gt;<em>Au Layer</em>: TFA&lt;br&gt;<em>Ti and SiO₂ Layer</em>: BHF</td>
<td></td>
</tr>
<tr>
<td>Step</td>
<td>Process Description</td>
<td></td>
</tr>
<tr>
<td>------</td>
<td>---------------------</td>
<td></td>
</tr>
</tbody>
</table>
| 10   | RIE: p-type layer  
     Gas: SF6  
     Pressure: $\sim 1 \times 10^{-3} \, \text{T}$  
     Power: 100W |
| 11   | Ion implantation  
     Ion: Boron  
     Energy: 30keV  
     Dose: $1 \times 10^{15} \, \text{cm}^{-2}$ |
| 12   | Remove mesa mask with wet etch  
     Au Layer: TFA  
     Ti and SiO$_2$: Layer: BHF |
| 13   | Anneal lattice damage from implantation  
     Temperature: 1050°C  
     Time: 90 minutes  
     Environment: Ar  
     Pressure: $\sim 1 \times 10^{-6} \, \text{T}$ |
| 14   | Photolithography of frontside contact mask  
     Photoresist: Positive (AZ-1518)  
     Develop: 5:1 (Water: AZ 351 Developer)  
     or 1:1 (Water: AZ Developer) |
| 15   | Deposit backside and frontside contacts  
     Method: E-Beam Evaporation  
     Backside Layer 1: 1500Å of Ni  
     Frontside Layer 1: 400Å of Ti  
     Frontside Layer 2: 1100Å of Al |
| 16   | Lift-off frontside contacts  
     Method: Acetone soak |
| 17   | Anneal contacts  
     Temperature: 1000°C  
     Time: 2 minutes  
     Environment: Ambient  
     Pressure: $1 \times 10^{-6} \, \text{T}$ |
| 18   | Photolithography of frontside contact mask  
     Photoresist: Positive (AZ-1518)  
     Develop: 5:1 (Water: AZ 351 Developer)  
     or 1:1 (Water: AZ Developer) |
| 19   | Deposit additional contact metal  
     Method: E-Beam Evaporation  
     Backside Layer 1: 100Å of Ti  
     Backside Layer 2: 5000Å of Ni  
     Frontside Layer 1: 5000Å of Al |
| 20   | Lift-off frontside contacts  
     Method: Acetone soak |
| 21   | Electrical Characterization  
     Method: I-V Probing |
<table>
<thead>
<tr>
<th>No</th>
<th>Title</th>
<th>Author</th>
<th>Dimension</th>
<th>Parameter</th>
<th>Value</th>
<th>Method</th>
<th>Advantage</th>
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<tr>
<td>1</td>
<td>SiC Semiconductor Devices Technology, Modelling, and simulation</td>
<td>Tesfaye Ayalew <a href="http://www.iue.tuwien.ac.at/phd/">http://www.iue.tuwien.ac.at/phd/</a></td>
<td></td>
<td>p+ thickness and concentration</td>
<td>0.5 μm, 1.0 x 10¹⁷ cm⁻³</td>
<td>Reactive ion etching (RIE)</td>
<td>SiC device technology for further modern electronics device</td>
</tr>
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<td></td>
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<td></td>
<td></td>
<td>n-epilayer thickness and</td>
<td>10.5μm, 7.2 x 10¹⁵ cm⁻³</td>
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<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>concentration</td>
<td></td>
<td></td>
<td></td>
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<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>n+ cathode thickness and</td>
<td>1.0μm, 1.0 x 10¹⁹ cm⁻³</td>
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<td>concentration</td>
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<td>2</td>
<td>Fabrication of a Silicon PIN Diode for Radiation Detection</td>
<td>H. G. Nam, M. S. Shin, K. H. Cha and N. I. Cho</td>
<td>Dimension: 3mm x 3mm</td>
<td>p+ thickness and concentration</td>
<td>1.0μm, 1.0 x 10¹⁹ cm⁻³</td>
<td>Photolithography, oxidation, ion implantation, aluminum sputter deposition</td>
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<td>n-epilayer thickness and</td>
<td>250μm</td>
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<td>n+ cathode thickness and</td>
<td>1.0μm, 1.0 x 10¹⁹ cm⁻³</td>
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<td>concentration</td>
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<td>3</td>
<td>Power handling capability of W-band INGAAS Pin diode switches</td>
<td>A. Egor, C. Delong &amp; P. Dimitrie</td>
<td>0.44 mm x 1.6 mm</td>
<td>p+ thickness and concentration</td>
<td>1.0μm, 1.5 x 10¹⁴ cm⁻³</td>
<td>The diode were fabricated using wet etching</td>
<td>Radar application for automotive industry,</td>
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<td>n-epilayer thickness and</td>
<td>1.0μm, 5 x 10¹⁵ cm⁻³</td>
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<td>n+ cathode thickness and</td>
<td>1.0μm, 1.5 x 10¹⁹ cm⁻³</td>
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<td>Method of operating PIN diodes and superlattice devices as far infrared detections</td>
<td>D.C Darryl, P.D, Robert, A.G. Unil Perera et.al</td>
<td>p+ thickness and concentration</td>
<td>0.2 – 3.0μm, 3.0 x 10^15 cm⁻³</td>
<td>(molecular beam epitaxy &amp; chemical vapor deposition)</td>
<td>Far infrared detector</td>
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<td>Low-Voltage SiGe Power Diodes</td>
<td>G.A.M. Hurkx, E.A. Hijzen, M.A.A. Zandt</td>
<td>p+ thickness and concentration</td>
<td>10 – 20 nm, 1.0 x 10^17 cm⁻³</td>
<td>Passivation - mesa etching n oxide passivation</td>
<td>To explore the limits of SiGe power diode technology</td>
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<td>n-epilayer thickness and concentration</td>
<td>3.0μm, 1.1 x 10^16 cm⁻³</td>
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<td>n+ cathode thickness and concentration</td>
<td>10 – 20nm, 1 x 10^17 – 10^18 cm⁻³</td>
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<td>A Novel Low-Frequency PIN diode</td>
<td>D.Loudmila</td>
<td>p+ thickness and concentration</td>
<td>5 x 10^19 cm⁻³</td>
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<td>Diode has multilayer structure possibility to operate at low frequencies</td>
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<td>n-epilayer thickness and concentration</td>
<td>5.0μm, 1.0 x 10^17 cm⁻³</td>
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<td>n+ cathode thickness and concentration</td>
<td>1.0 x 10^20 cm⁻³</td>
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<td>Silicon carbide devices for advanced, high efficiency power conversion.</td>
<td>C.Michael</td>
<td>p+ thickness and concentration</td>
<td>1.16μm, 5 – 6 x 10^17 cm⁻³</td>
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<td>To know the suitable criteria for PIN diode like power dissipation and cooling requirement</td>
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<td>n-epilayer thickness and concentration</td>
<td>6μm, 5 – 6 x 10^15 cm⁻³</td>
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<td>n+ cathode thickness and concentration</td>
<td>395μm, 5 – 6 x 10^15 cm⁻³</td>
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<td>8</td>
<td>Microwave PIN diodes for GaAs IC</td>
<td>R.Tayrani, M.I. Sobhy</td>
<td>p+ thickness and concentration</td>
<td>3 µm, $1 \times 10^{18}$ cm$^{-3}$</td>
<td>Microwave application</td>
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<td>n- epilayer thickness and concentration</td>
<td>2 µm, n$^-$ $1 &lt; 10^{12}$ cm$^{-3}$</td>
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<td>n+ cathode thickness and concentration</td>
<td>2 µm, $1 \times 10^{18}$ cm$^{-3}$</td>
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<td>9</td>
<td>Thermal Annealing n propagation of shockley stacking fault in 4H-SiC PiN Diodes</td>
<td>D.C. Joshua, X.L.Kendrick, J.T.Marko et.al</td>
<td>Active area: 1.2 mm$^2$</td>
<td>p+ thickness and concentration</td>
<td>2 - 3 µm, $1 \times 10^{18}$ cm$^{-3}$</td>
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<td>n- epilayer thickness and concentration</td>
<td>100 µm, $5 \times 10^{14}$ cm$^{-3}$</td>
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<td>n+ cathode thickness and concentration</td>
<td>300 µm, $1 \times 10^{16}$ cm$^{-3}$</td>
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<td>For further development of a driving force mechanism</td>
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<td>10</td>
<td>characteristics of 6H-Silicon Carbide PIN diodes Prototyping by laser doping</td>
<td>Z.Tian, N.R. Quick &amp; A.Kar</td>
<td>Active area: 3mm x 3mm</td>
<td>p+ thickness and concentration</td>
<td>430 µm, Al: $2 \times 10^{21}$ cm$^{-3}$</td>
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<td>n- epilayer thickness and concentration</td>
<td>430 µm, Al: $2 \times 10^{21}$ cm$^{-3}$</td>
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<td>n+ cathode thickness and concentration</td>
<td>430 µm, Al: $2 \times 10^{21}$ cm$^{-3}$</td>
<td>Laser doping technique</td>
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<td>Direct-write laser can be used to fabricate prototype PIN diode</td>
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2.6 Chapter Summary

The background and device physics of PIN diode has been further explained in this chapter. Apart of the device physics, the important parameter of PIN diode also discussed as they will be considered and applied for the simulations and verification process. On the other hand, the parameter for the switching speed performance is also clarified. The last part of this chapter listed down various steps involve in the fabrication process. The process basically varies depends on the PIN diode device structure and application. From the literature review, the device structure is designed and all the parameter discussed are considered in the study. The methodology carried out in Chapter 3 adopt these important parameters to simulate the device structure.
REFERENCES


"http://www.paper.edu.nc/, Fabrication and Characteristics of Thick PIN Detector", Austin, TX, 2000