A NEW D-PISO ARCHITECTURE FOR DYNAMIC SYMBOL SIZE DIGITAL BASEBAND MODULATION IMPLEMENTATION IN FPGA

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To everyone who supports me, it just begins...

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ABSTRACT

Dynamic symbol size modulation is a type modulation which could provide a fast transmission speed by removing the redundant symbol as compare to fixed symbol size modulation. The dynamic nature of the symbol created an additional problem in hardware design as the size of symbol needed to be defined clearly and it cannot be change and altered once the design has been generated. Thus, to address the issue, this research investigated the best implementation method and performance study of fixed and dynamic symbol size digital baseband modulation for optical communication system in FPGA hardware design. KCU105 FPGA development board and Vivado software were chosen as the main platform to implement the design. A new architecture to implement dynamic symbol size baseband modulation in FPGA is presented in this thesis. Clock control (CC) is used as the research's based design to create two new architectures which use multiple parallel in serial out (M-PISO) and dynamic parallel in serial out (D-PISO). Next, by using D-PISO architecture, dynamic symbol size modulation namely 8-reverse dual header pulse interval modulation (8-RDHPIM), 8-digital pulse interval modulation (8-DPIM) and fixed symbol size modulation 8-pulse position modulation (8-PPM) were fully implemented in the FPGA which has a transmitter and receiver module. An experimental comparative study was then carried out for each modulation technique. The main parameters investigated were data timing analysis, hardware utilization, power utilization as well as bit error rate performance. From the results, it can be concluded that for power limited system, 8-PPM could be selected as it can maintain a small number of symbol error rate (SER) even during low power transmission which is around -6 dBm. On the other hand, the 8-DPIM and 8-RDHPIM that achieved the transmission speed of 33.3 Mbps and 27.27 Mbps are suitable for systems that require high data speed and minimal clock synchronization.

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ABSTRAK

Modulasi simbol saiz dinamik adalah modulasi yang berkebolehan untuk menghasikan transmisi data yang pantas iaitu dengan mengurangkan simbol berlebihan seperti yang ada pada modulasi simbol size tetap. Namun begitu, simbol saiz dinamik sukar dilaksanakan dalam rekabentuk fizikal kerana saiz simbol harus dinyatakan dengan jelas dan tidak boleh diubah selepas dihasilkan. Oleh itu, penyelidikan ini mengkaji berkenaan pelaksanaan dan prestasi modulasi digital jalur asal yang mempunyai saiz simbol yang tetap dan dinamik bagi sistem komunikasi optik. *FPGA KCU105* dan perisian Vivado dipilih sebagai platform utama dalam kajian ini. Reka bentuk baru untuk melaksanakan modulasi dinamik saiz simbol jalur asal ke dalam FPGA telah dibentangkan dalam tesis ini. Dengan menggunakan kawalan jam (*CC*) sebagai reka bentuk asas, dua bentuk rekaan menggunakan pelbagai masukan selarian - keluaran siri (*M-PISO*) dan dinamik masukan selarian - keluaran siri (*D-PISO*) telah dikaji. Seterusnya, menggunakan reka bentuk D-PISO, modulasi dinamik saiz simbol seperti modulasi 8-tajuk dwi terbalik selang denyut digital (8-RDHPIM), modulasi 8-selang denyut digital (*8-DPIM*) dan modulasi 8-kedudukan denyut (*8-PPM*) dilaksanakan sepenuhnya pada FPGA tersebut dimana terdiri dari modul pemancar dan penerima. Kajian perbandingan eksperimen kemudian dijalankan bagi setiap teknik modulasi. Parameter utama kajian adalah analisis data masa, penggunaan perkakasan, penggunaan kuasa serta prestasi kadar ralat. Daripada hasil dapatan kajian, kami dapat menyimpulkan bahawa untuk sistem kuasa terhad, *8-PPM* boleh digunakan kerana ia dapat mengekalkan jumlah kadar ralat yang kecil walaupun pada pancaran kuasa rendah iaitu dalam lingkungan -6 *dBm*. Dalam pada itu, *8-DPIM* dan *8-RDHPIM* pula mecatat kelajuan transmisi sebanyak 33.3 *Mbps* and 27.27 *Mbps* yang mana sesuai digunakan untuk sistem yang memerlukan kelajuan data lebih tinggi dan penyeragaman jam yang minima.

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LIST OF SYMBOLS AND ABBREVIATIONS

CC	-	Clock Control
DPIM	-	Digital Pulse Interval Modulation
D-PISO	-	Dynamic Parallel In Serial Out
FPGA	-	Field Programmable Gates Array
Laser	-	Light Amplification by Stimulated Emission of Radiation
LED	-	Light Emitting Diode
M-PISO	-	Multiple Parallel In Serial Out
PD	-	Photodiode
PER	-	Packet Error Rate
PPM	-	Pulse Position Modulation
RDHPIM	-	Reverse Dual Header Pulse Interval Modulation
SSL	-	Solid State Lighting

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CHAPTER 1

INTRODUCTION

In recent years, digital modulation with dynamic symbol size has been investigated especially regarding pulse time modulation [1]–[3]. Dynamic symbol size is the term used to define modulated signal symbol that changes depending on the input data which are usually found in pulse time modulation technique [4],[5]. Table 1.1 shows the comparison of symbol size for 8-pulse position modulation (PPM), 8-digital pulse interval modulation (DPIM) and 8-reverse dual header- pulse interval modulation (RDHPIM) with respect to 3 bit on-off keying (OOK) input.

Table 1.1: Baseband modulation data symbol [3], [5], [7]

OOK	8-PPM	8-DPIM	8-RDHPIM
000	10000000	10	011
001	01000000	100	0111
010	00100000	1000	01111
011	00010000	10000	011111
100	00001000	100000	001111
101	00000100	1000000	00111
110	00000010	10000000	0011
111	00000001	100000000	001

PPM is the modulation that changes transmitted data by changing a single bit 1 (pulse) position within transmission period (T). A fixed 2^n time slots is created during the transmission period which directly dependents on the number of input bit size (n). This is repeated every T seconds and as such that the transmitted bit rate is calculated in M/T bits per second. The 8-PPM requires a fixed eight (8) bit symbol size to represent the three (3) input bit [6]. On the other hand, PIM is the modulation that changes the interval and symbol size according to the input data. The 8-DPIM for

instance, increases the symbol size by adding bit 0 as the input sequence increases [2]. In this particular example, a symbol size between 2-9 bit is required to represent the input data. The 8-RDHPIM further reduces the symbol size to 3-6 bits by introducing a two (2) bit header to the initial symbol structure. The header is used as a starting bit as well as a symbol indicator for each symbol. It helps to remove the dependency for a synchronous clock between a transmitter and receiver system which eases the implementation of a design especially for independent system [4]. With these modulation refinements, higher data rates and bandwidth efficiency could be achieved. Theoretically, any modulation with dynamic symbol size such as PIM could provide a major improvement to the PPM system. However, it is difficult for the system to be implemented in a hardware design as the platform does not support a dynamic array register unlike if it is done in a software design.

An optical transmission system usually contains the hardware components as shown in Figure 1.1. The components are pseudorandom binary sequence (PRBS), modulator, laser, medium channel, demodulator, and symbol error rate (SER). PRBS is used to generate input bit to be transmitted [8]–[10]. A modulator is used to modulate the raw data into modulated signal. Laser then converts the modulated signal into optical signal. A medium is the channel used to transmit the optical signal. A photo-detector is used to revert the optical signal into electrical signal. Sampling is used to sample the electrical signal into raw data. A demodulator is used to interpret the sample data to actual data. SER is then used to compare the transmitted data with received data to determine the error rate. In an actual experiment, each component has to be set up using a particular hardware. PRBS is created using PRBS generator module. Modulator, sampling, demodulator and SER are created using a modular circuit. laser module as light source and light sensor as photo detector is used to support transmission channel using fibre or free space. This set up requires a lengthy step and some spaces to keep the hardware. This method is also inflexible especially for electrical components that are used for a pre made circuit.

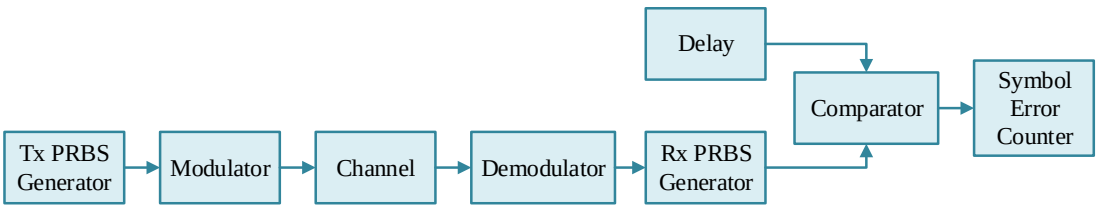

Figure 1.1: Basic transmission structure [11-12]

The developments in semiconductor and computing field have made it possible to simplify the optical communication system by transforming all the electrical components in a single chip implementation [11]–[13]. Contemporary field-programmable gate arrays (FPGAs) have large resources of logic gates and RAM blocks to implement complex digital computations [11]. As FPGA designs employ very fast I/O rates and bidirectional data buses, it becomes a challenge to verify a correct timing of valid data within setup time and hold time [14]. Floor planning enables resource allocation within FPGAs to meet these time constraints. FPGAs can be used to implement any logical function that an ASIC could perform [15]. The ability to update the functionality after shipping, partial re-configuration of a portion of the design and the low non-recurring engineering costs relative to an ASIC design offer advantages for many applications [16].

1.1 Problem Statement

The dynamic symbol size modulation is a relatively old concept. However, dynamic symbol size modulation digital baseband transmission such as PIM has not been extensively addressed in hardware design and experimental works. Most of the research found are in mathematical and simulation stages. A key challenge for this type of modulation is to implement the dynamic symbol size into the system efficiently. Time is a major concern in creating a robust communication system [7]. All modulations need some sorts of synchronisation to achieve successful transmissions [17]. Although software-based implementation is promising , it is not a feasible platform for a physical layer such as optical transmission system [11]. The problem originates from the architecture of the processor itself that is totally dependent on coding/instruction-driven implementation which supports only one instruction that can be executed in a single clock cycle [18]. Depending on the instruction style and size, an unwanted delay within the system emerges during the implementation. The delay causes the transmission system in experiencing instability during data flow and this could potentially create massive data loss during transmission [12]. A hardware based implementation using FPGA is chosen to implement the design since the timing and synchronization issues can be solved using this platform. The FPGA however, creates another challenge as it does not directly support dynamic array unlike during

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software-based implementation [15]-[19]. In this research, a new architecture is created to implement the dynamic modulation efficiently in the FPGA hardware design. Based on the new architecture, an experimental study is then carried out as a proof of concept to compare between the fixed and dynamic modulations. The finding of this research would permit further implementations of dynamic modulation in future applications.

1.2 Research Objectives

In order to achieve the purpose of this study, which is to investigate the performance of digital implementation in FPGA, the researcher embarks on the following objectives:

i) To design a new multiple-parallel input serial output (M-PISO) and dynamic-parallel input serial output (D-PISO) architecture that could support a dynamic array which in turn can support a dynamic symbol size digital baseband modulations for FPGA hardware design using Vivado software in Verilog language.
ii) To implement the fixed and dynamic symbol size modulation hardware architecture which includes the transmitter and receiver modules into the FPGA platform.
iii) To analyse the performance of the implemented modulations on a FPGA board in terms of data rates, hardware utilisation, power analysis, timing summary, and symbol error rate.

1.3 Research Scopes

The research scopes are presented as follow:

i) The maximum M-level of modulation is limited only to 8. As the research work only focuses to verify the new architecture, 8 level modulation is sufficient for the task.
ii) Real hardware implementation of the proposed architectures are deployed on the Xilinx KCU105 FPGA. It is notable that the proposed designs and

implementations are platform independent, and can be implemented easily on the most recent FPGAs. Moreover, by using the resources available on the recent platforms, a better performance can be achieved. However, due to time and funding limitations, real implementations on these platforms are unable to be carried out.

1.4 Limitation of Existing Work and Research Opportunity

There are still remains a huge gap for further research in exploiting the dynamic symbol size implementation.

Three major limitation of the existing work can be identified as follows:

i) Dynamic symbol size modulation digital baseband transmission such as PIM has not been extensively addressed in experimental work as shown in timeline in Figure 1.2. For the past years, most of the studies have focused on different variants of dynamic symbol size modulation technique equation and software simulation which aim for higher speed and lower power consumption.

ii) Dynamic symbol size modulation technique is still cannot be implemented efficiently especially in FPGA hardware design. Although there are DPIM designs that have been successfully implemented in FPGA, they are not suitable to be used for other variants of application. From the review, a very limited FPGA-based implementation has been found that is related to dynamic modulation, and interestingly there has been only 1 discussion reported for the implementation using dynamic symbol size modulation. Therefore, the design and implementation of dynamic modulation algorithm and architecture create a strategic and very promising opportunity.

iii) New architecture for implementing Dynamic symbol size modulation in FPGA is required to be created. As HDL such as VHDL and Verilog do not support any dynamic array declaration during run time, a different method is needed to implement the modulation that uses single clock based architecture to synchronise all data flow within the design.

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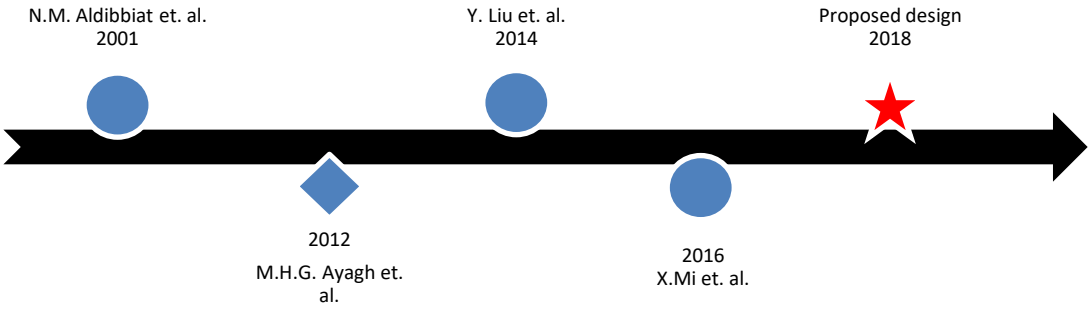

Figure 1.2: Timeline summary for dynamic symbol size modulation previous research [134-137]

Based on the existing work limitations, the objectives of the research works presented in this thesis can be summarized as follows:

i) Design and implement a new architecture for dynamic symbol size baseband modulator using a series of algorithms that are implemented in Verilog;
    1. Create the appropriate formulation for M-PISO and D-PISO to be used in Verilog HDL.
    2. Evaluate both architectures and select the best method for further development.

ii) Design and implement the fixed and dynamic modulation hardware architecture which includes the transmitter and receiver module into the FPGA platform.
    1. Create the appropriate formulation for fixed modulation (PPM) based current architecture and dynamic modulation (DPIM and RDHPIM) based on the selected architecture which consists of transmitter and receiver modules to be used in Verilog HDL.
    2. Evaluate and compare the architectures implemented in FPGA in terms of timing and power consumption.

iii) Experimental works of the implemented architectures with free space optical communication using laser and photo detector as the transmission medium.
    1. Create a formulation for Verilog testbed for performance analysis that consists of comparator and symbol error rate (SER) module.
    2. Design the free space optical system medium using laser and photo detector

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3. Evaluate the performance of symbol error rate (SER) for all modulations in terms of power transmission and data speed.

1.5 Research Contributions

Figure 1.3 shows the overall research strategies and contributions that have been achieved in this research. Firstly, two architectures called multiple - parallel input serial output (M-PISO) and dynamic- parallel input serial output (D-PISO) with clock control algorithms to support dynamic symbol size modulation is presented. Secondly, using D-PISO based algorithms, Pulse Position Modulation (PPM), Digital Pulse Interval Modulation (DPIM) and Reverse Dual Header Pulse Interval Modulation (RDHPIM) modulator and demodulator algorithm is implemented in FPGA. Finally, the experimental work is carried out for all modulations. The algorithm performances are then compared to exhibit another noteworthy analysis and discussion in terms of Symbol Error Rate (SER), clock synchronisation as well as the hardware implementation design.

1.6 Thesis Organisation

The structure of the remaining thesis is as follow. Chapter 2 takes a closer look at the most recent architectures and systems for digital modulation implementation in FPGAs as well as recent development in optical communication research. Next, Chapter 3 covers the methodology in term of design, implementation and performance study of new algorithms that implement a dynamic symbol size modulation in FPGAs. In Chapter 4, It covers the results of behavioral and timing of the algorithms. Last but not least, Chapter 5 provides the concluding remarks and possible improvements of the current research are highlighted. Finally, possible future research directions in the design and implementations of dynamic symbol size modulation are presented

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