SIMULATION, FABRICATION AND CHARACTERIZATION OF NMOS TRANSISTOR

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To my parents; for your love and support

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ABSTRACT

This thesis explains the recipe module development for the first Long Channel NMOS transistor device fabrication process at cleanroom laboratory of KUiTTHO. A recipe for the NMOS transistor fabrication process has been successfully produced. Threshold Voltage and Leakage Current, with different channel length and oxide gate for the Long Channel NMOS transistor too has been investigated. The data from the experiment conducted have shown that the threshold voltage is more influenced by the thickness of the oxide gate as compared with the channel length. The threshold voltage increased in linear form with the increase of the oxide gate thickness; and there is almost no change for different channel length. Leakage Current reduces exponentially with the increase of the oxide gate thickness and the channel length.

ABSTRAK

Tesis ini menerangkan pembangunan modul resepi bagi proses fabrikasi peranti transistor kesan medan logam-oksida semikonduktor salur panjang (*Long Channel NMOS transistor*) yang pertama kali di makmal bilik bersih KUiTTHO. Resepi bagi proses fabrikasi peranti transistor kesan medan logam-oksida semikonduktor telah berjaya dihasilkan. Voltan ambang dan arus bocor salir, dengan panjang salur dan oksida get yang berbeza bagi transistor kesan medan logam-oksida semikonduktor salur panjang telah di kaji. Data dari eksperimen yang telah dilakukan menunjukkan voltan ambang banyak di pengaruhi oleh ketebalan oksida get berbanding dengan panjang salur. Voltan ambang naik secara *linear* dengan kenaikan ketebalan oksida get dan hampir tidak ada perubahan bagi panjang salur yang berbeza. Arus bocor salir berkurangan secara eksponen dengan kenaikan ketebalan oksida get dan panjang salur.

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LIST OF SYMBOLS

A	Area
Å	Symbol for 10^{-10}cm or 10^{-8}m
c	Speed of light in vacuum
C	Capacitance
C_j	Junction capacitance per unit area
C_{ox}	Oxide capacitance per unit area
D	Diffusion coefficient
E	Electric field
E_a	Acceptor energy
E_c	Conduction band energy of a semiconductor
E_d	Donor energy
E_F	Fermi energy (thermal equilibrium)
E_g	Energy bandgap of a semiconductor
E_i	Intrinsic Fermi energy Joule
E_v	Valence band energy of a semiconductor
F_n	Quasi-Fermi energy of electrons
F_p	Quasi-Fermi energy of holes
h	Plank's constant
I	Current
J	Current density
J_n	Electron current density
J_p	Hole current density
k	Boltzmann's constant

L	Length
m	Mass
n	Electron density
n_i	Intrinsic carrier density
N	Doping density
N_a	Acceptor doping density
N_c	Effective density of states in the conduction band
N_d	Donor doping density
Q	Charge
$Q_{p.B}$	Hole charge in the base
Q_d	Charge density per unit area in the depletion layer of an MOS structure
$Q_{d.T}$	Charge density per unit area at threshold in the depletion layer of an MOS structure
R	Resistance
t	Thickness
t_{ox}	Oxide thickness
T	Temperature
v	Velocity
v_{th}	Thermal velocity
V_a	Applied voltage
V_B	Base voltage
V_D	Drain voltage
V_B	Body voltage
V_G	Gate voltage
Vt	Thermal voltage
V_{TH}	Threshold voltage
x_d	Depletion layer width
xd,T	Depletion layer width in an MOS structure at threshold
x_j	Junction depth
x_n	Depletion layer width in an n-type semiconductor
xp	Depletion layer width in a p-type semiconductor

ε_{ox}	Dielectric constant of the oxide F/m
ε_s	Dielectric constant of the semiconductor F/m
μ_n	Electron mobility
μ_p	Hole mobility
Φ_M	Workfunction of a metal V
Φ_{MS}	Workfunction difference between a metal and a semiconductor V

CHAPTER I

PROJECT OVERVIEW

1.1 Overview

This chapter will explain the project overview and scopes of project.

1.2 Introduction

The history of microelectronics began on December 1947 at the Bell Labs, United States of America, when three scientists John Brdeen, Wafter Brattain and William Shockley invented the first semiconductor device which is called the transistor that was able to replace the functions of the vacuum tube as an amplifier. The said invention had opened the path in producing electronic circuitry designs that were small and cheap. Entailing the discovery, large numbers of electronics companies were incorporated including one by William Shockley himself in the year 1955 in Santa Clara

Valley near San Francisco. Miniaturizing of electronics circuitry was made by assemblying the transistors and other components onto the printed circuit board (PCB) that interconnects the components.

In 1965, Gordon Moore had predicted that total number of transistors in a chip would doubled in every 12 months period. His prediction has become a polar of probablity and prediction. This prediction is known as "Moore's Law" [9]. Figure 1.1 shows the formula towards Moore's Law that gives an enormous impact to the developing world of the semiconductors and microelectronics today.

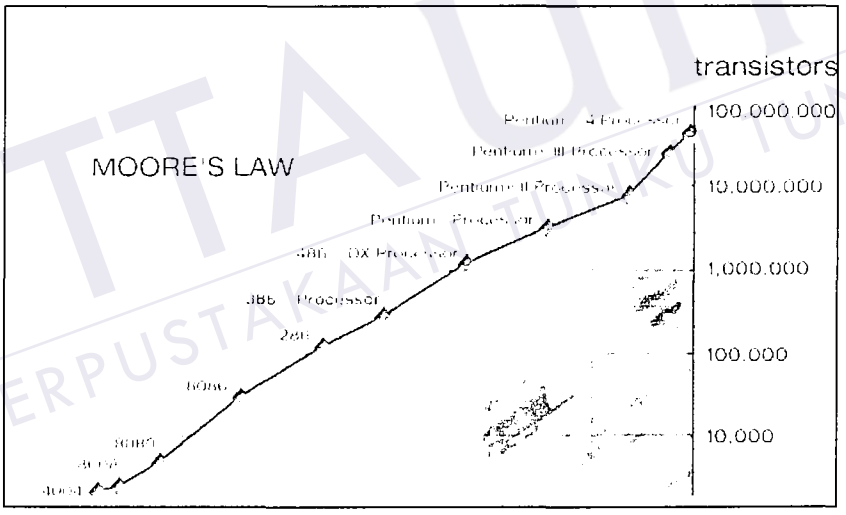

Figure 1.1 Prediction Formula of *Moore's Law*

Subsequence to the prediction made by Gordon Moore through Moore's Law, the fabrication technology of the integrated circuits were experiencing evolutions starting from the Small Scale Integration - SSI, Medium Scale Integration - MSI, Large Scale Integration - LSI, Very Large Scale Integration - VLSI and Ultra Large Scale Integration - ULSI [13].

In line with the development of this fabrication technology, the Semiconductor Industry Association (SIA) has issued a prediction schedule relating to the current technology development and the future one. Table 1.1 shows the technology development predictions encompassing the minimum size of transistor that can be fabricated on an integrated circuit chip. Size of this transistor is measured based on the parameter known as the channel length.

Based on the Table 1.1, it can be seen that the transistors size is expecting shrinkage from year to year and subsequently increases the number of transistors onto a chip. This matter is spurred by the size scaling of its component. The scaling of transistor ssize which has caused the size of the transistor to become smaller has in fact enable the switching time for a transisitor to decrease and subsequently enhances the operation speed of a transistor. Briefly it can be said that, the shrinking of the transistor size can enhance the speed of a transistor.

Table 1.1 Technology Development Forecast By Semiconductor Industry Association (SIA)

	Year					
	1999	2001	2003	2006	2009	2012
Channel Length (um)	0.14	0.12	0.1	0.07	0.05	0.035
Transistor /cm^2 (million)	14	16	24	40	64	100
Die Size (mm^2)	800	850	900	1000	1100	1300

1.3 Problem Aspire

The development of microelectronic field which occurs today has given rise to competition among companies to produce transistor device which has excellent features. This in turn has made the fabrication process recipe becomes confidential. Thus, each clean room laboratory should develop its own recipe.

The reduction in threshold voltage is widely used as an indicator of evaluating technology. A lower threshold voltage means less power supplies and faster circuits. The threshold Voltage value for the NMOS transistor changes depending on the process and design parameters.

As transistor size continues to scale down, leakage current has become a critical issue of the integrated circuit design. Leakage current not only contributes to total power, but also leads to system performance.

1.4 Objectives

The project objectives are as follows:

1. To study the threshold voltage with different oxide gate thickness and channel length for Long Channel NMOS transistor.

2. To study the drain leakage current with different oxide gate thickness and channel length for Long Channel NMOS transistor.

3. To produce a recipe for NMOS transistor fabrication for Micro Fabrication Cleanroom of KUiTTHO.

1.5 Project Scope

This project encompasses two sections of work that were:

1. Design and conduct a simulation for long channel NMOS transistor by using ISE TCAD in the Advanced Digital Electronic Laboratory of KUiTTHO. The simulated transistor has different channel length and oxide gate thickness.

2. Conduct fabrication of long channel NMOS transistor with different channel length and oxide gate thickness in the clean laboratory of KUiTTHO.

3. Conduct analysis for NMOS transistor characteristics obtained through simulation and fabrication.

CHAPTER II

LITERATURE REVIEW

2.1 Introduction

A transistor is an important device in the electronic circuit. It can function as an amplifier to boost the power, voltage or the current. Transistors too have been used as switches in the digital circuits and the computers.

Basically, the transistors can be divided into two main groups that are the bipolar and unipolar transistors. A bipolar transistor or in short the BJT (Bipolar Junction Transistor) uses both the electron and hole as the carrier. The BJT operation is controlled by the current. This is because of the out flowing current is depends on the inflow current.

The Field Effect Transistor – FET uses only the electron or the hole as the carrier while the FET operation is being control by the voltage. The voltage which exists at the gate will control the current that is flowing through the device [14]. In brief, the transistor family can be presented by the following Figure 2.1.

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