DESIGNING OF AN OPERATIONAL AMPLIFIER

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To **my darling husband**... *Md. Nazri Mohidin @ Mohyeddin*... you are all things beautiful to me...

To **my adorable kids**... *Mirza Khumaini, Nuqman Nazhan, Firas Nazih and Naqib Nadzif*... you are always in my heart and will always be...

To **my beloved father**... *Haji Timyati Alwai*... I really appreciate your upbringing and endless support...

To **my only sister**... *Noor Fahrina Timyati*... may you lead a successful life despite your hearing disability...

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ABSTRACT

Natural signals come in analog forms and these signals are bearing valuable information and need to be processed. An operational amplifier is the most versatile and important building blocks in analog circuit design. Therefore this project is dedicated to designing an operational amplifier and analyzing the properties. The performance is measured based on its DC and small-signal analysis. Schematic of the circuit is drawn using Tanner EDA's S-Edit™. Then T-Spice™ is utilized to simulate the circuit. Output waveform generated by W-edit is used to obtain the DC curve, the Bode plot for magnitude and Bode plot for phase. Additionally, other types of parameters are used for the same circuit. It is found that Level 1 Parameters suits the operational amplifier being designed and it works well as expected. The design gives a 96dB gain. The layout for the whole circuit is done based on MOSIS layout rules using SCN3M technology.

ABSTRAK

Dunia kita dipenuhi oleh pelbagai isyarat analog semulajadi yang membawa maklumat-maklumat tertentu. Namun maklumat ini perlu diproses sebelum digunakan. Salah satu komponen yang paling berguna dan merupakan salah satu blok penting dalam rekabentuk litar analog ialah penguat operasi. Oleh itu, projek ini adalah bertujuan untuk menghasilkan litar penguat operasi dengan mengambilkira pelbagai faktor penting dalam rekabentuk litar. Hasil simulasi litar ini digunakan untuk menentusahkan semua kiraan yang dibuat semasa proses rekabentuk. Prestasi litar diukur berdasarkan analisis DC dan isyarat kecil. Litar skematik dalam projek ini dihasilkan menggunakan S-Edit™ Tanner EDA. Simulasi litar pula menggunakan T-Spice™. Gelombang keluaran dilihat melaui W-Edit dan kemudiannya digunakan untuk menentukan kemampuan litar. Sebagai tambahan, penggunaan set parameter yang berlainan turut digunakan untuk simulasi litar yang sama. Hasil kajian mendapati rekabentuk litar ini sesuai menggunakan parameter Level 1 dan dapat beroperasi seperti yang dikehendaki. Litar yang direka menghasilkan gandaan sebanyak 96dB. Bentangan keseluruhan litar juga telah dibuat berdasarkan hukum bentangan dari MOSIS menggunakan teknologi SCN3M.

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CHAPTER I

INTRODUCTION

The chapter is dedicated to description of background of the problem with statement of the problem is then clarified. Then, the expected findings, objectives, importance and scope of project are explained. Relevant terms used are revealed in the last part of this chapter.

1.1 Background of the Problem

Digital implementation offers significant benefits. The operation of digital circuits does not require precise values of the signal and this means digital circuits are less sensitive than analogue circuits. Moreover, the emergence of very large-scale integration (VLSI) circuits had enabled the integration of complex digital signal processing (DSP) systems on a single chip. In terms of storage, digital signal can be stored almost indefinitely on various media without any loss (Mitra, 2006). These advantages had made digital implementation much more desirable than its analogue counterpart.

As most natural signals are in analogue form, including the biomedical signals, analogue signals need to be converted into digital form to be processed digitally. Sampling is a crucial step in typical digital signal processing system (Floyd, 2006).

Apparently, development of the integrated circuits in microelectronics industry is the most influential industry in the society. Operational amplifiers are one of the devices that could be designed using metal-oxide semiconductor field-effect transistors (MOSFET) in microelectronics analogue circuit design (Howe & Sodini, 1997). Sampling circuits also employ operational amplifier in its building blocks.

A simple sample-and-hold (S/H) circuit consists of an input buffer, an electronic switch, a storage capacitor and an output buffer as in Figure 1.1. The switch is closed during sample mode enabling V_{out} to track input voltage. In the hold mode, the switch is opened, isolating the storage capacitor from the input and V_{out} remains until the next sampling phase. Traditionally, S/H circuits are in voltage-mode whereby input voltage is sampled at discrete-times and held constant until the next sampling instant (Chennam & Fiez, 2004).

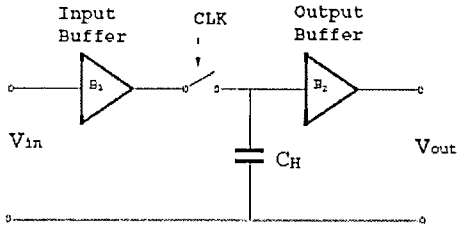

Figure 1.1: Simple sample-and-hold (Chennam & Fiez, 2004).

1.2 Statement of the Problem

Technology scaling and reduced supply voltages results in increased speed and reduced power consumption. Low power consumption is favourable in complementary metal-oxide semiconductor (CMOS) designs because this could prolong the battery-life. Therefore, this project is focusing in designing an operational amplifier with low voltage supply and low power consumption.

1.3 Expected Findings

The project is meant to come up with an operational amplifier to be used in analogue-to-digital converter (ADC) circuit. In this project, integrated circuit design system will be used. Therefore it consists of the schematic of transistor level circuits and their respective simulated output waveforms. Outputs will be obtained through the schematic editor, SPICE simulator and waveform viewer. The performance of the operational amplifier in this project is determined by its direct current (DC) characteristics and frequency response. All the values are first obtained by calculation and then compared with simulation values.

1.4 Objectives

The output of the project is an operational amplifier consists of Metal Oxide Semiconductor (MOS) transistors. Specifically, the project purposes are:

1. To design an operational amplifier with power supply of 3.3V.
2. To design an operational amplifier that dissipates power in milli-Watts range.

1.5 Importance of the Study

This project is a CMOS analogue electronic design of an operational amplifier. It will have a relatively high gain at lower frequencies. An operational amplifier with good DC characteristics will eliminate the need of a voltage offset in the circuit and thus reduce the complexity of the circuit. Low power consumption in operational amplifier is desirable and therefore, this project will concentrate on producing an operational amplifier that consumes less power.

1.6 Scope of Project

There are many types of operational amplifier available. The operational amplifier in this design is set to:

1. Use power supplies of V_{DD} = 3.3V and V_{SS} = -3.3V.
2. Dissipate power in milli-Watt range.
3. Have the minimum length of 3μm for all transistors.
4. Drive a typical capacitive load of 7.5pF for operational amplifier.

1.7 Thesis Outline

This thesis started with Chapter I whereby every introduction that briefly describes the project. Then, Chapter II reveals the previous works on operational amplifier and all the theories relevant to design an operating amplifier. The research methodology is included in Chapter III. All the calculation and simulation results of the operational amplifier are in Chapter IV. As the final chapter, Chapter V includes discussion, conclusion, and recommendation.

CHAPTER II

LITERATURE REVIEW

2.1 Literature Review

In order to facilitate comparison, the results obtained from previous works that had been published are summarized in Table 2.1. The operational amplifier concept is then briefly discussed. This project used MOSFETs, thus, the designation of voltages and currents are clarified first. Then, the drain characteristics of MOSFETs are pointed out. Equations related to the DC analysis of the amplifier are introduced and also equations involved in the small-signal analysis of the operational amplifier.

2.1.1 Previous Works

Operational amplifier design has been developed continuously. The previous works can be concluded as in Table 2.1.

Table 2.1: Results of operational amplifier in the previous research works.

	Author	Year	Power Supply (V)	Architecture	Low Freqency Gain (dB)	Unity Gain Frequency (Hz)	Phase Margins (degrees)	Power Dissipation (W)
1	Rob van Dongen & Vincent Rikkink	1995	1.5V	simple two-stage	63dB	1MOhm|150pF = 0.85MHz 1kOhm|150pF = 1.1MHz	1MOhm|150 pF = 47deg 1kOhm|150pF = 59deg	135uW
2	G.N. Lu & G. Sou	1998	1.3V	regulated-cascode	>68dB	10MHz (transition frequency)	70deg	0.28mW
3	Kimmo Lasanen, Elvi Riiisiinen-Ruotsalainen & Juha Kostamovaara	2000	1.0V	bulk-driven Miller comp.	83dB	190kHz	73deg	5uW
4	Jean-Francois Delage & Mohamad Sawan	2001	2.7-5.0V	two-stage	91.8dB	>13.8MHz	>51deg	not available
5	Vadim I-Vanov & Shilong Zhang	2002	2.5-5.5V	not available	>100dB	250MHz	not available	not available
6	Franz Schlögl & Horst Zimmermann	2005	1.2V	4-stage Miller comp.	128.8dB	693MHz	48deg	18mW
7	Carsten Bronskowski & Dietmar Schroeder	2006	3.3V	rail-to-rail folded cascode	not available	1.1-39MHz	>55deg	140uW-30mW
8	Philipp Meier auf der Heide, Carsten Bronskowski, Jakob M. Tomasik & Dietmar Schroeder	2007	3.3V	programmable operational amplifier based on rail-to-rail	not available	0.3-48MHz (μ power consumption)	68.4deg	49uW

Power consumption is one of the critical aspects in operational amplifier design. As power consumption is directly related to the current and voltage supply, it seems that reduced supply voltages means reduced power consumption. The low frequency gain and unity-gain frequency are two other aspects usually discussed. Process integration refers to the well-defined collection of semiconductor processes required to fabricate CMOS integrated circuits. There is a strong connection between circuit design and process integration (Baker, 2005). Since operational amplifiers in this review are all CMOS integrated circuit, variation in process might lead to variation in performance of the operational amplifier.

Rob van Dongen and Vincent Rikkink (Dongen & Rikkink, 1995) had developed two-stage architecture for the operational amplifier. The input stage was a transconductance amplifier while the output stage is a common-source amplifier. The combination has poles at higher-frequencies which were at 0.85 MHz and 1.1 MHz. Common-source amplifier was chosen for the output stage because it can operate using as low as 1V of voltage supply since in this configuration, there will be no more than two transistors between the V_{DD} and ground.

Likewise, Jean-Francois Delage and Mohamad Sawan (Delage & Mohammad Sawan, 2001) were also proposing an operational amplifier based on two-stage amplifier. However, this operational amplifier was developed by a rail-to-rail input stage and an AB class amplifier at the output. It has minimal phase margin with 35pF of capacitive load. The pole is situated at 13.8 MHz. This means that the amplifier has a higher frequency of unity gain apart from having a higher low-frequency gain than the operational amplifier proposed by Ron van Dongen and Vincent Rikkink.

Similarly for this project, two-stage architecture is proposed for the operational amplifier, as it will meet the desired specification.

2.2 MOSFET

The metal-oxide semiconductor field-effect transistor, MOSFET is a multi-terminal microelectronic device. MOSFETs are the dominant transistor type for digital IC's and have important applications in analogue signal processing circuits (Howe & Sodini, 1997).

2.2.1 MOSFETs Designations

An understanding of the symbols of MOSFET, particularly the voltage and current designations, is important in discussing the current-voltage characteristics. These are featured in Figure 2.1. MOSFET is a four terminal device with interchangeable drain and source. However, the simplified three terminals model are the most often used with consideration that the substrate is grounded (or most negative voltage, V_{SS}) or well is tied to V_{DD}. This is important in performing simulations through Tanner EDA Tools.

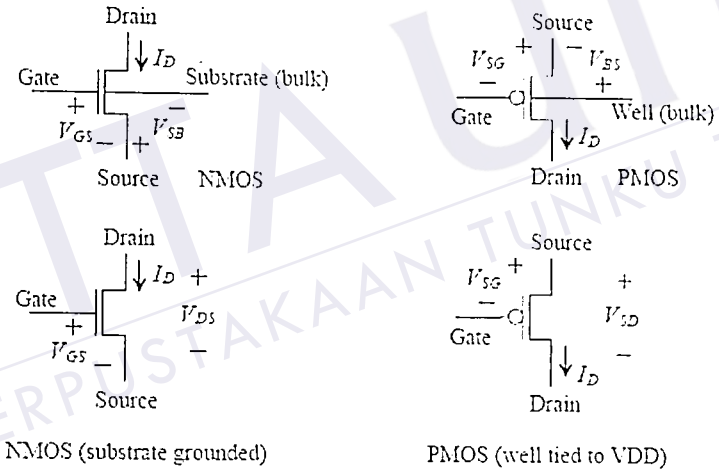

Figure 2.1: Voltage and current designations for MOSFETs (Baker, 2005).

2.2.2 MOSFET Drain Characteristics

The MOSFET's DC characteristics are often discussed in terms of its drain current, I_D functional dependence on the two voltages: the gate-source voltage, V_{GS} and the drain-source voltage, V_{DS} (Howe & Sodini, 1997). Graphically, these characteristics are plotted in an I-V curve. MOSFET could be in triode region, which it will act like a voltage-controlled resistor. It could also be in saturation region, which means the MOSFET is functioning more as a current source. The I-V curves and the description are as in Figure 2.2.

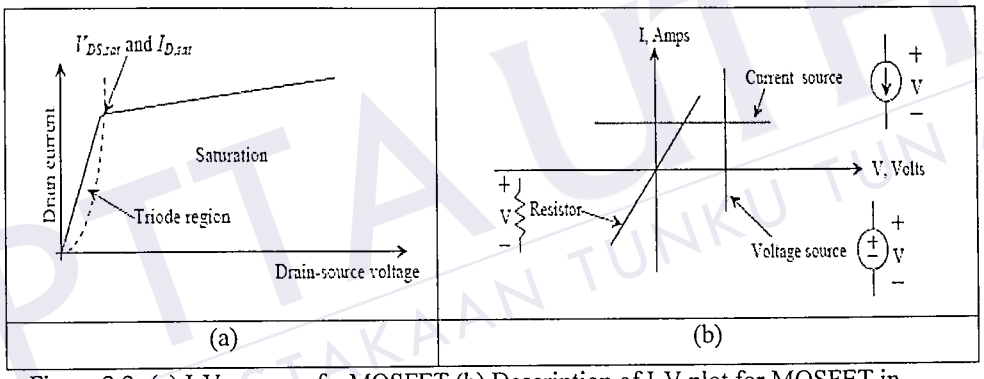

Figure 2.2: (a) I-V curves of a MOSFET (b) Description of I-V plot for MOSFET in simpler words (Baker, 2005).

An example of drain-current characteristics of an n-channel MOSFET (NMOS) and p-channel MOSFET (PMOS) with its test circuit is shown in Figure 2.3 and Figure 2.4 respectively. The MOSFET is cutoff when drain current, $I_D = 0A$ and the gate-source voltage is smaller than its threshold voltage, $V_{GS} < V_T$. Typical value of V_T is 1V. Once the drain-source voltage becomes larger than the difference between gate-source voltage and threshold voltage, $V_{DS} > V_{GS} - V_T$, I_D is nearly independent. This is the saturation region whereby the MOSFET behaves almost like a current source. In the triode region, I_D depends on both V_{GS} and V_{DS} (Howe & Sodini, 1997).

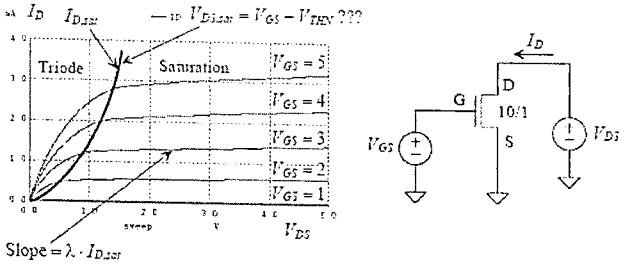

Figure 2.3: Characteristics of an NMOS device (Baker, 2005).

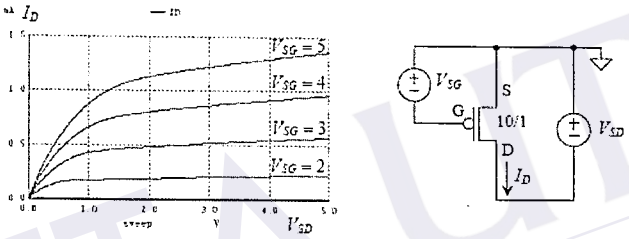

Figure 2.4: Characteristics of a PMOS device (Baker, 2005).

2.2.3 MOSFET Circuit Model

Steady-state equations for I_D as a function of the terminal voltages are important in finding the steady-state behaviour of digital circuits and for biasing analogue amplifiers. MOSFET's in analogue designs are usually biased in saturation region. Therefore, small-signal model in the saturation region is valuable. The steady-state equations for n-channel MOSFET are as in Table 2.2.

Table 2.2: Steady-state equations for n-channel MOSFET.

Region	*NMOS*	
	Current	***Voltage***
Cutoff	$I_D = 0A$	$V_{GS} \leq V_{Tn}$
Linear/ Triode	$I_D = \frac{\mu_n C_{ox} W}{L}\left(V_{GS} - V_{Tn} - \frac{V_{DS}}{2}\right)(1 + \lambda_n V_{DS})V_{DS}$	$V_{GS} \geq V_{Tn}, V_{DS} \leq V_{GS} - V_{Tn}$
Saturation	$I_{D_{SAT}} = \frac{\mu_n C_{ox} W}{2L}(V_{GS} - V_{Tn})^2(1 + \lambda_n V_{DS})$	$V_{GS} \geq V_{Tn}, V_{DS} \geq V_{GS} - V_{Tn}$

The drain current equations for p-channel MOSFET, is derived the same way with n-channel MOSFET. However, the drain voltage is negative with respect to the source and the drain current is also negative. Therefore, the steady-state equations for p-channel MOSFET are as in Table 2.3.

Table 2.3: Steady-state equations for p-channel MOSFET.

Region	*PMOS*	
	Current	***Voltage***
Cutoff	$-I_D = 0A$	$V_{SG} \leq -V_{Tp}$
Linear/ Triode	$-I_D = \frac{\mu_p C_{ox} W}{L}\left(V_{SG} - V_{Tp} - \frac{V_{SD}}{2}\right)(1 + \lambda_p V_{SD})V_{SD}$	$V_{SG} \geq -V_{Tp}, V_{SD} \leq V_{SG} - V_{Tp}$
Saturation	$-I_D = \frac{\mu_p C_{ox} W}{2L}(V_{SG} - V_{Tp})^2(1 + \lambda_p V_{SD})$	$V_{SG} \geq -V_{Tp}, V_{SD} \geq V_{SG} - V_{Tp}$

The average electron mobility of the channel is represented by μ_n and oxide capacitances are C_{ox}. In this project, MOSFET is simulated using the simplest level

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