SIMULATION STUDIES OF 30 MHz PHASE-LOCKED LOOP COHERENT RECEIVER

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ABSTRACT

Phase-Locked Loop or in short PLL is a vital part in electronics system mainly in communication system in getting back the transmitted signal. As a whole, it is basically a closed loop frequency control system where its function is based on the phase sensitive detection of phase difference between the input signal (transmitted signal) and the output of the controlled oscillation. Although the system had been around since 1930's, implemented by the French Engineer, H. De Bellescise, but still, until today further development is in progress in achieving better response and performance in retrieving and synchronising transmitted signals. The purpose of this project is to familiarise in designing and constructing a 30 MHz Phase-Locked Loop Coherent Receiver by computer simulation, taking account the requirements for each building block of a PLL system, the stability of the system and the response of the system. To achieve this, the process includes simple and direct calculations, and circuit simulations observation. Results are represented in graphs and are analysed.

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CHAPTER I

INTRODUCTION

1.1 History

Phase-Locked Loop has been implemented by a French Engineer in 1932. This system replaced several other receiver system inventions, namely the super heterodyne radio receiver and later the homodyne or synchrodyne receivers. The "old" radio receivers first invented in 1918 by E. H. Armstrong while serving the Army Signal Corps in France. These classic designs consist of local oscillator, a mixer and audio amplifier. Their basic concept of operation was when the input signal and local oscillator were mixed at the same phase and frequency, the output was an exact audio representation of the modulated carrier.

It was considered a perfect system initially, but then the synchronous reception became difficult due to tiny drift in frequency of the local oscillator after a period of time in operation. Phase-Locked Loop is an evolution to solving oscillator problems. The key to the successful system is providing correction voltage feedback (or also known as Error Voltage signal) to the oscillator from the phase detector and thus keeping it on the right frequency. Although the homodyne or synchrodyne receivers seemed superior to the super heterodyne receivers, the cost of constructing

Phase-Locked Loop circuit outweighed its advantages that made the Phase-Locked Loop became more popular among designers and manufacturers.

In 1940's, the first commonly usage of Phase-Locked Loop was in the synchronisation of the horizontal and vertical sweep oscillators for television system. Since then, the electronic phase-locked loop principle has been extended to other applications. AM and FM Demodulators, FSK Decoder, Touch-Tone® Decoder, motor speed controller, Robotics and Radio Control transmitter and receivers. In the wireless world, Phase-Locked Loop is used for

1. Carrier Synchronisation
2. Carrier Recovery
3. Frequency division and multiplication
4. Demodulation

The first Phase-Locked Loops were analogue but since 1970's, integrated circuits have been available to perform the same functions on a chip. These are called digital PLLs. There are 4 different types of PLLs.

1. The Linear or Analogue PLL (LPLL)
2. The Digital PLL (DPLL)
3. The All-Digital PLL (ADPLL)
4. Software PLL (SPLL)

The concept basis behind each of the first three is the same. They are specified by the same standard parameters such as loop bandwidth and damping factor. But Software PLL is usually implemented by a microcontroller, microcomputer or digital signal processor (DSP), it is generally considered to be an all-digital and it can perform like a LPLL, a DPLL or and ADPLL. Therefore SPLL is the most universal

type of PLL but the limitation is, it needs computer algorithm performing the PLL function to be executed at least once in every period of the input signal of the PLL.

1.2 Aim

The purpose of this project is to familiarise with designing of a Phase Locked-Loop system and as a guide, the focus is on a 30MHz coherent receiver.

1.3 Importance of Studies

The project benefits is to adopting and gaining the experience of designing a Phase-Locked Loop system by the practical approach and employ some fundamental knowledge and theories. And also engineer them in building the basic blocks of a Phase Locked-Loop system.

CHAPTER II

BACKGROUND

2.1 Reviews

Since the system had been invented over the past 70 years, a lot of articles and books had been written by numerous authors. Among them, Garth Nash, an Application Engineer in his "Phase-Locked Loop Design Fundamental", Application Note, Motorola Inc 1994. He concluded and described the basic control techniques required for Phase-Locked Loop design. He also presented the criteria for selection of the optimum type of loop and methods for establishing the desired performance characteristics.

Books written by R. E. Best in "Phase-Locked Loop, Design, Simulation and Applications", 3rd edition, McGraw Hill,1997 and "Phaselock Technique", by F. M. Gardner, 2nd edition, 1979, John Wiley & Sons, New York provides crucial and important theories in designing the Phase-Locked Loop system although they were deeply describing the operation of a Phase Locked-Loop system.

And, Mark Curtin and Paul O' Brien in their "Phase-Locked Loops for High-Frequency Receivers and Transmitters Part 1,2 & 3" Analog Dialog 1999, emphasised the phase noise, reference spurs and output leakage current. Perhaps this can be adopted to the 30 Mhz Phase-Locked Loop system design as their conclusion were based on high frequencies system.

2.2 Scope

The scope of this project is to study and design a 30 MHz Phase-Locked Loop coherent receiver by computer simulation, looking into requirements, response and behaviour for each individual building block of the Phase-Locked Loop.

CHAPTER III

OBJECTIVE

To support the aim of this project, these are the objectives identified.

1. To study the behaviour of the individual building block of the Phase-Locked Loop system i.e. The Phase Detector, the Loop Filter and the Voltage Controlled Oscillator.

2. To calculate the circuit requirements using the right formulas to achieve the response of each building block circuit for the 30 MHz Phase-Locked Loop coherent receiver.

3. Simulate each circuit design of the building block of the Phase-Locked Loop and their combinations. At this stage, make changes or modification if necessary to the design.

CHAPTER IV

METHODOLOGY

The designing uses direct approach in assembling them. By looking into the response of each basic building block, and the observations pursued onto the overall system response. In the first stage, simple calculations were made for the required components values. Secondly, constructing the circuit for each building block of the Phase-Locked Loop for computer simulations and analysing the behaviour and response of each building block of the Phase-Locked Loop.

Having the advantages and capability to add non-existence components to its library, MultiSIM ™ & Electronics Workbench ™ (MultiSIM 2001 Education Version) had been chosen. The components' parameters and Spice Models can be easily obtained from the respective manufacturers.

4.1 The Architecture Design

The basic building of a Phase Locked-Loop is shown in Figure 4.1.

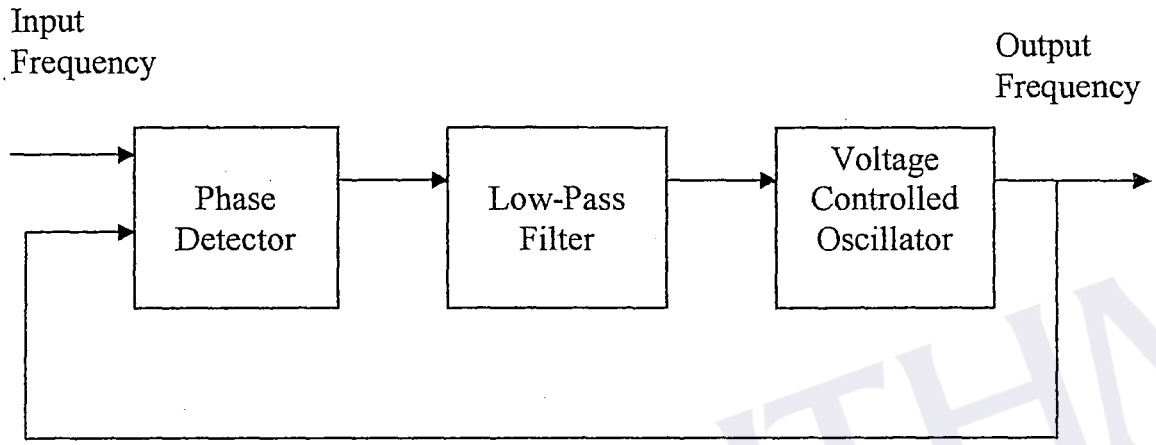

Figure 4.1 Basic Building Block of Phase-Locked Loop

4.2 The Phase Detector

In linear Phase-Locked Loop, the Phase Detector is actually a four-quadrant multiplier and a gain value is also associated with it. The phase Detector compares two input frequencies, generating an output that is the measure of the phase difference. (If they differ in frequency, it gives a periodic output at difference frequency).

In other words, the Phase Detector produces voltages that are proportional to the phase difference between input signal and the signal of the Voltage Controlled

Oscillator. These voltages, after being filtered, are used as feedback, to control the Voltage Controlled Oscillator oscillation.

The basic construction of the circuit employed was the Gilbert Multiplier Cell shown in Figure 4.2 with an added current source to ensure the gain control (provided by Rg) and DC biasing control (provided by Rbs) for the circuit. This had become an advantage of having the freedom to control the overall response and performance of system at later.

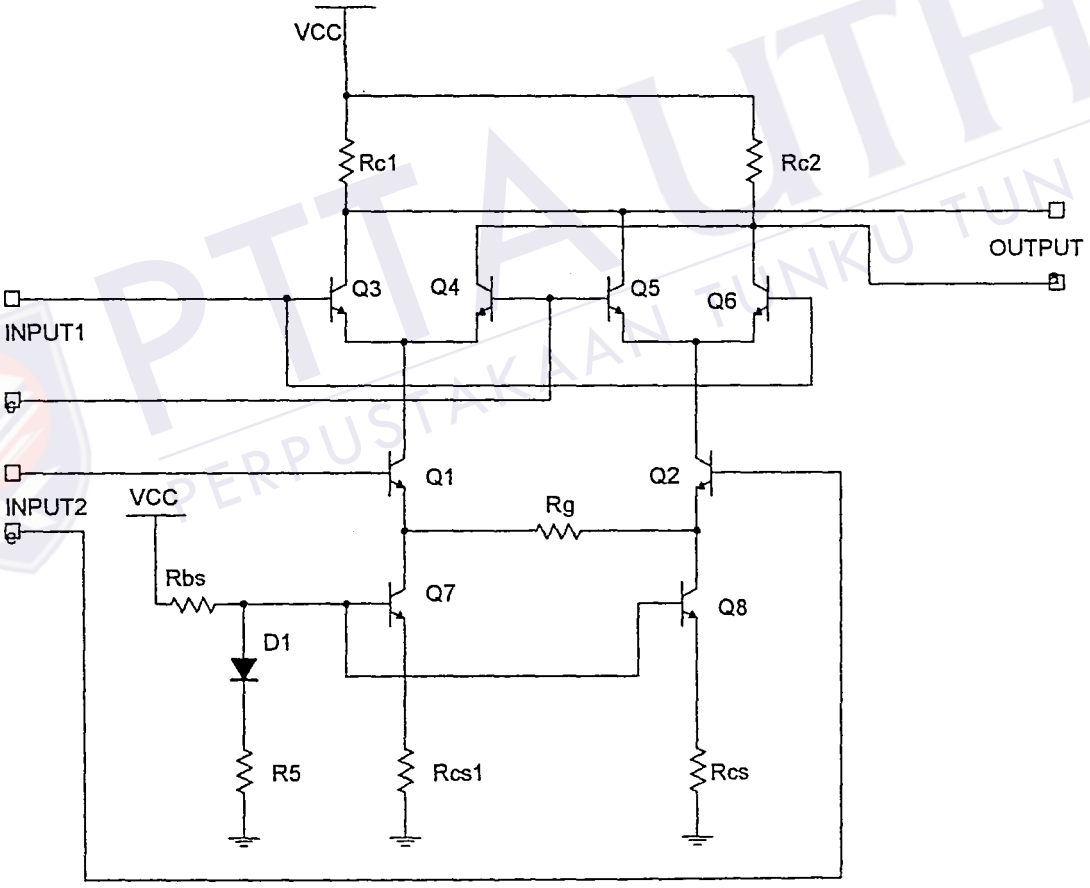

Figure 4.2 The Gilbert Multiplier Cell

4.3 The Low-Pass Filter (Loop Filter)

The basic loop filter was built from a Low-Pass passive or active filter. In most designs, Linear Phase-Locked Loop utilises First Order Low Pass Filter although many will assume there are other higher order filters which may have difficulties in achieving system stability. The components values were calculated with respect to the required cut-off frequency and tested in the computer simulation along with the Phase Detector.

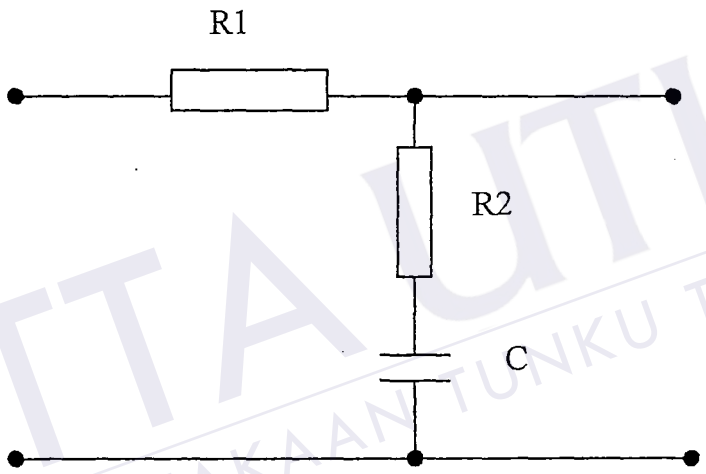

Figure 4.3 The Low-Pass Filter (Loop Filter)

4.4 The Voltage Control Oscillator

Basically, a Voltage Controlled Oscillator is a variable frequency oscillator and is made to change frequency by changing the value of one of the frequency determining circuits. If the input frequency is not the same to Voltage Controlled Oscillator frequency, the phase error signal, after being filtered causes the Voltage Controlled Oscillator to deviate in the direction of the input frequency. If the

conditions are right the Voltage Controlled Oscillator will quickly locked to the input frequency, maintaining a fixed relationship with the input signal but within its range.

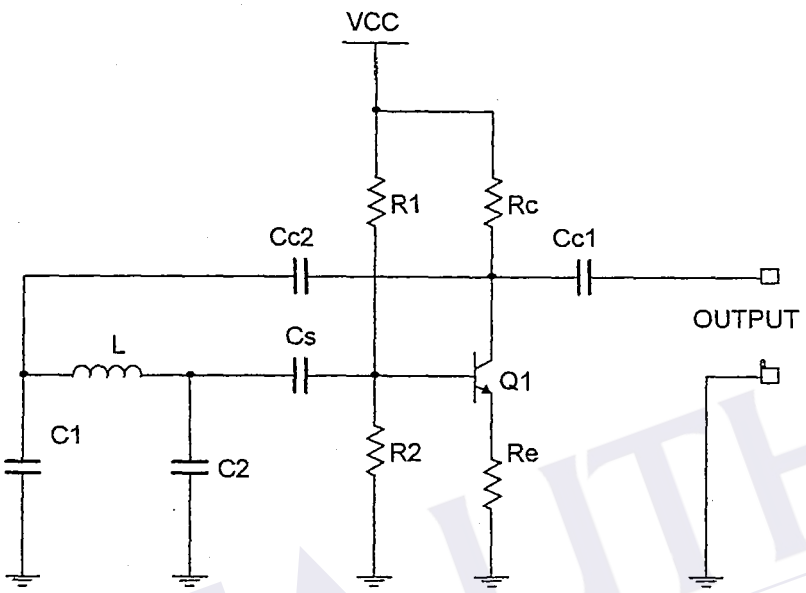

Figure 4.4 The Colpitts Oscillator Circuit

The Colpitts Oscillator consists of a CE amplifier and a tank circuit. The reason for choosing CE amplifier was that, CE amplifier is known for its stability and such that the oscillator is the crucial and critical element for the success of the system design. Furthermore, Colpitts Oscillator architecture possesses two capacitors in the tank circuit (L, C1 and C2) which later they were changed to varactors that made it a Voltage Controlled Oscillator. And again simple calculation is made in determining the components for oscillation.

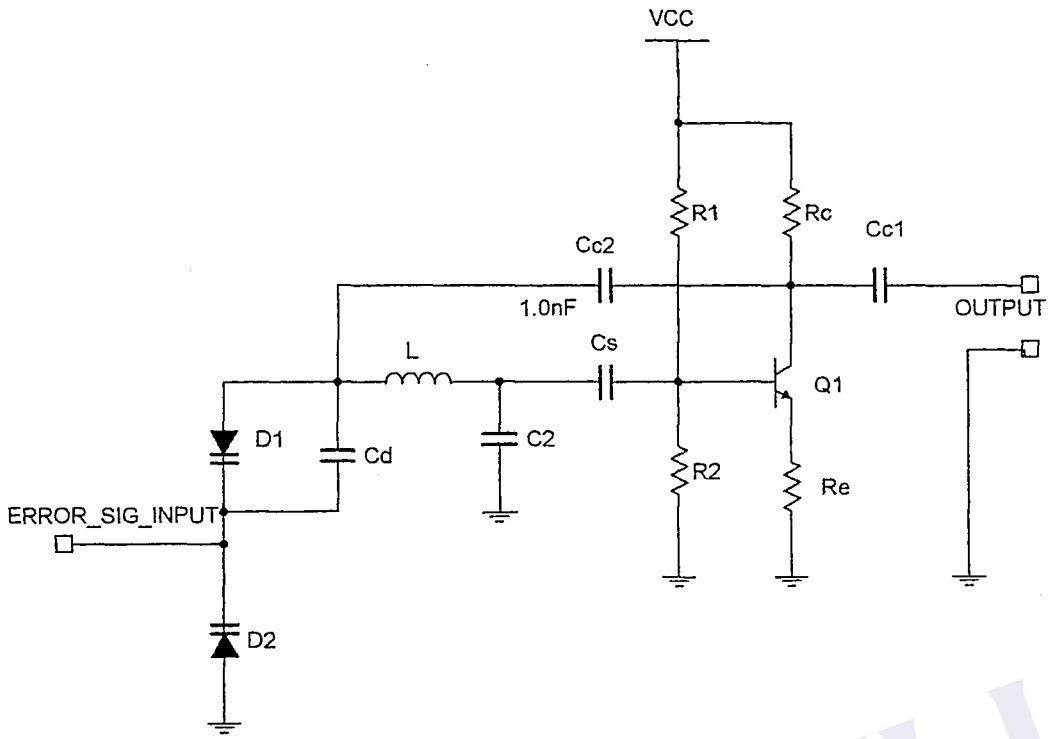

Figure 4.5 The Voltage Controlled Oscillator Circuit

After observations on response of each building block, all the circuits were combined and analysed.

CHAPTER V

RESULTS & DISCUSSIONS

5.1 The Low-Pass Filter (Loop Filter)

Referring to Figure 4.3, the basic formulas are used for the determination of the components values are as follows where Wc1 and wc2 are the cut-off frequency.

$$Wc2 = \frac{1}{CR2}$$

$$R2 = \frac{1}{2\pi fcC}$$

$$R2 = \frac{1}{2(30x16^{6})(39x10^{-12})}$$

$$R2 = 136\Omega$$

The Preferred Value is 130Ω

$$Wc1 = \frac{1}{C(R1 + R2)}$$

$$R1 = \frac{1 - 2\pi fcCR2}{2\pi fcC}$$

$$R1 = \frac{1 - (2\pi)(30x10^{6})(39x10^{-12})(130)}{2\pi(30x10^{6})(39x10^{-12})}$$

$$R1 = 6.02\Omega$$

The Preferred Value is 6.2 Ω

5.2 Oscillation Determination

By using the formula

$$Wo = \sqrt{\frac{C1 + C2}{(L)(C1)(C2)}}$$

And assuming C1=C2=C. The formula becomes

$$Wo = \sqrt{\frac{2C}{(L)(C^{2})}}$$

Rearranging the equation

$$C = \frac{2}{(L)(Wo^{2})}$$

Where Wo = $2\pi f$ and assuming L = 1 μH, obtained C = 56.3 pF (the preferred value is 56 pF). Although from the Barkhausen criteria requires C2 = C1 (at least) so that voltage gain Av = 1 for oscillation, where $Av = -\frac{C2}{C1}$, it is an added advantage of having C2 ≥ C1.

Therefore, the chosen values are C2 = 62 pF and C1 = 51 pF and Voltage Gain of 1.22 obtained with these combination.

5.3 Amplifier Circuit Design

As for the amplifier circuit, begin with the Rc. Let Rc = 2 kΩ.

$$RE = \frac{Rc}{Av}$$

$$RE = \frac{2x10^3}{1.22}$$

$$RE = 1.64x10^3\,\Omega$$

The Preferred Value is 1.6 kΩ

The base resistance is,

Rb = 0.1βRE (where β = 75 for transistor 2N2222A)

Rb = $0.1(75)(1.6x10^3)$

Rb = 12 kΩ.

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