IMPLEMENTATION OF LUO-RUDY PHASE I CARDIAC CELL EXCITATION MODEL IN FPGA

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For my beloved family and
to everyone who supports me, it just begins…

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ABSTRACT

Dynamic simulation of complex cardiac excitation and conduction requires high computational time. Thus, the hardware techniques that can run in the real-time simulation was introduced. However, previously developed hardware simulation requires high power consumption and has a large physical size. Due to the drawbacks, this research presents the adaptation of Luo-Rudy Phase I (LR-I) cardiac excitation model in a rapid prototyping method of field programmable gate array (FPGA) for real-time simulation, lower power consumption and minimizing the size. For the rapid prototyping, a nonlinear Ordinary Differential Equation (ODE)-based algorithm of the LR-I model is implemented by using Hardware Description Language (HDL) Coder that is capable to convert MATLAB Simulink blocks designed into a synthesisable VHSIC Hardware Description Language (VHDL) code and verified using the FPGA-In-the Loop (FIL) Co-simulator. The Xilinx FPGA Virtex-6 XC6VLX240T ML605 evaluation board is chosen as a platform for the FPGA high performance system which is supported by the HDL Coder. A fixed-point optimisation has been successfully obtained with Percentage Error (PE) and Mean Square Error (MSE) which are -1.08% and 2.28%, respectively. This result has given better performance for the hardware implementation in terms of 27.5% decrement in power consumption and 5.35% decrement in utilization area with maximum frequency 9.819 MHz. By implementing the constructed algorithm into the high performance FPGA system, a new real-time simulation-based analysis technique of cardiac electrical excitation has been successfully developed.

ABSTRAK

Simulasi dinamik pengujaan dan pengaliran jantung yang kompleks memerlukan masa pengiraan yang tinggi. Oleh itu, teknik-teknik perkakasan yang boleh dijalankan dalam simulasi masa nyata telah diperkenalkan. Walau bagaimanapun, simulasi perkakasan yang dibangunkan sebelum ini memerlukan penggunaan kuasa yang tinggi dan mempunyai saiz fizikal yang besar. Oleh kerana kelemahan tersebut, penyelidikan ini mempersembahkan penyesuaian model pengujaan jantung Luo-Rudy Fasa I (LR-I) dalam kaedah prototaip pantas bagi tatasusunan get boleh atur cara medan (*Field Programmable Gate Array*: FPGA) untuk simulasi masa nyata, penggunaan kuasa yang lebih rendah dan pengurangan saiz. Untuk prototaip pantas, model LR-I berasaskan algoritma persamaan pembezaan biasa tidak linear dilaksanakan dengan menggunakan *Hardwre Description Language* (HDL) *Coder* yang mampu untuk menukar blok MATLAB Simulink yang direka ke dalam kod *VHSIC Hardware Description Language* (VHDL) dan disahkan menggunakan *FPGA-In-Loop* (FIL) *Co-simulator*. Papan Penilaian Xilinx FPGA Virtex-6 XC6VLX240T ML605 dipilih sebagai platform untuk sistem FPGA berprestasi tinggi yang disokong oleh HDL Coder. Pengoptimuman titik tetap telah berjaya diperolehi dengan Ralat Peratusan (RP) dan Ralat Min Kuasa Dua (RMKD) yang masing-masing -1.08% dan 2.28%. Keputusan ini telah memberikan prestasi yang lebih baik untuk pelaksanaan perkakasan dari segi 27.5% susutan dalam penggunaan kuasa dan 5.35% susutan dalam kawasan penggunaan dengan frekuensi maksimum 9.819 MHz. Dengan melaksanakan algoritma yang dibina ke dalam sistem FPGA berprestasi tinggi, teknik analisis baru pengujaan elektrik jantung berasaskan simulasi masa nyata telah berjaya dibangunkan.

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LIST OF PUBLICATIONS

Journal:

1. **N. Othman**, F. Mahmud, A. K. Mahamad, M. Hairol Jabbar, N. A. Adon, "Voltage-clamp simulation of cardiac excitation: field programmable gate array (FPGA) implementation," *ARPN Journal of Engineering and Applied Sciences 2016*. Vol. 11. no 24. pp. 14056-14064. ISSN 1819-6608.

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LIST OF SYMBOLS AND ABBREVIATIONS

$[Ca]_i$ - inner cell calcium ion concentration
$[K]_i$ - inner cell potassium ionconcentration
$[K]_o$ - outer cell potassium ion concentration
$[Na]_i$ - inner cell sodium ion concentration
$[Na]_o$ - outer cell sodium ion concentration
Δt - time discretization step
C - membrane capacitance
clk_enb - input to start the system operation
d - activation gate of slow inward current
E - Nernst potential of ion channel
F - Faraday constant
f - inactivation gate of slow inward current
g - conductance of ion channel
G - maximum conductance of ion channel
h - inactivation gate of sodium
I_b - background current
I_{ext} - external stimulation current
I_{ion} - summation of all ion currents
I_K - time-dependent potassium current
I_{K1} - time-independent potassium current
I_{kp} - time-independent plateau potassium current
I_m - membrane current
I_{Na} - fast sodium current
I_{si} - slow inward current
j - inactivation gate of sodium
$K_{1\infty}$ - inactivation gate
K_p - inactivation gate

m - activation gate of sodium
PR_{NaK} - permeability ratio
R - gas constant
T - absolute temperature
V_m - membrane voltage
V_{max} - fast upstroke velocity
X - activation gate of time-dependent potassium
X_i - inactivation gate of time-dependent potassium
α - opening rate constants of gate
β - closing rate constants of gate
1-D - One-Dimensional
2-D - Two-Dimensional
3-D - Three-Dimensional
AP - Action Potential
APD - Action Potential Duration
ASCII - American standard code for information interchange
ASIC - Application Specific Integrated Circuits
AV - Atria ventricle
BER - Bit Error Rate
B-R - Beeler and Reuter
CiPA - Comprehensive In Vitro Proarrhythmia Assay
CLB - Configurable Logic Block
CM - Courtemanche
CMOS - Complementary metal oxide semiconductor
CORDIC - Coordinate Rotation Digital Computer
CPU - Computer Processing Unit
DAC - Digital Analog Converter
DEPE - differential equation processing element
DSP - Digital Signal Processing
dsPIC - Digital Signal Peripheral Interface Controller
EEPROM - Electrically Erasable Programmable Read-only Memory
FBDF - Agilent technologies fast binary data format
FF - Flip Flop

FHN	- FitzHugh-Nagumo
FIL	- FPGA-in-the-Loop
FL	- Fraction length
FPAA	- Field Programmable Analog Array
FPGA	- Field Programmable Gate Array
FPU	- Floating-point unit
GPP	- General Purpose Processor
GPU	- Graphical Processing Unit
GUI	- Graphical User Interface
HDL	- Hardware Description Language
I/O	- Input/Output
IC	- Integrated Circuit
ICON	- Integrated Controller
ILA	- Integrated Logic Analyser
IOB	- Input/Output Block
ISE	- Integrated Software Environment
ISim	- ISE Simulator
I-V	- Current-Voltage
JTAG	- Joint test action group
LAB	- Logic Array Block
LC	- Logic Cell
LE	- Logic Element
LR-I	- Luo-Rudy Phase I
LUT	- Look-up Table
MHz	- Mega Hertz
MSE	- Mean Squared Error
MUX	- Multiplexer
NCD	- Native Circuit Description
NGD	- Native Generic Database
ODE	- Ordinary Differential Equations
PAR	- Place and Route
PC	- Personel Computer
PCI	- Peripheral Component Interconnect

PE - Percentage Error
PE - Processing Element
RAM - Read-only Memory
RK-4 - Runge-Kutta forth order
ROM - Random-access Memory
RTL - Register Transfer Level
SA - Sinoatrial
SIPHER - Scalable Implementation of Primitives for Homomorphic Encryption
SNR - Signal to Noise Ratio
SoC - System-on-Chip
SVPWM - space vector pulse width modulation
UCF - user constraint file
USB - Universal Serial Bus
VCD - value change dump
VHDL - Very High Speed Integrated Circuit (VHSIC) Hardware Description Language
VHM - Virtual Heart Model
VIO - Virtual Input/Output
VLSI - Very Large Scale Integration
WL - Word length
XSG - Xilinx System Generator

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CHAPTER 1

INTRODUCTION

1.1 Overview

This thesis examines the simulation study of a cardiac cell mathematical model on hardware implementation. Specifically, this study is to improve understanding of a cardiac excitation mechanism by reproducing quantitatively the action potential generation and phase-locked response to periodic current pulse stimulation by using high performance Field Programmable Gate Array (FPGA) implementation for Luo-Rudy Phase I (LR-I) model.

Section 1.2 discussed on the research background of cardiac excitation, while, section 1.3 summarised the problem statement that has been reported by previous studies which include large scale of variables, massive amounts of computational time, and challenges in writing the Hardware Description Language (HDL) code manually that lead to error prone, time consuming and high level languages that are difficult to be understood by non-FPGA experts, and the solution to these problems also are proposed. Besides, section 1.4 presents the research objectives, while section 1.5 explained the research scope and limitations. Lastly, the overall research contribution is discussed in section 1.6 and the thesis organisation is presented in 1.7.

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