AN OPTIMUM DESIGN OF A TWO-STAGE OPERATIONAL AMPLIFIER USING CARBON NANOTUBE FIELD-EFFECT TRANSISTOR AT 10 NM TECHNOLOGY NODE

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For my beloved mother and father,

Yai Chai May and Chua Kim Siong

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Dr. Chessda Uttraphan A/L Eh Kan

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ABSTRACT

The shrinking of the metal oxide semiconductor field-effect transistor (MOSFET) technology nodes to the deep-nanometre size leads to serious short-channel effects. Among the various technologies and device structures that have been proposed, the carbon nanotube field-effect transistor (CNFET) is the most promising candidate to replace the MOSFET. The effect of the structural parameters of CNFET on the two-stage operational amplifier (op-amp) performance is one of the active research areas in studying the CNFET when scaling down the CNFET based circuit from a larger technology node to a smaller technology node. This research investigates the CNFET structural parameters which are the number of tubes (N), the carbon nanotube (CNT) diameter (D_{CNT}), and the CNT pitch (S) to optimize the design of 32 nm and 10 nm two-stage CNFET op-amps. The op-amp circuits are optimized by balancing the open-loop gain, unity-gain bandwidth (UGB), power dissipation, and output resistance to obtain the optimum structural parameters. The optimized 10 nm two-stage op-amp is then compared with 32 nm to evaluate the optimum structural parameters and circuit performances. The evaluated circuit performances consist of open-loop gain, UGB, power dissipation, output resistance, input common-mode range (ICMR), common-mode rejection ratio (CMRR), power-supply rejection ratio (PSRR), slew rate, and settling time. Furthermore, this research also investigates the effect of S on the CNFET drain current (I_{CNFET}) when migrating from 32 nm to 10 nm technology node. Simulation results show that the optimum design of the 10 nm two-stage op-amp has successfully improved the performance of the 32 nm circuit by more than 33% for all the performance metrics. The performance metric that improved the most is UGB, which increased by 109.99%. The investigation of the impact of S on the I_{CNFET} when the size of the CNFET is reduced to 10 nm technology node suggests that the S parameter should be taken into account in the 32 nm I_{CNFET} equation for accurate drain current estimation. On the other hand, for simplicity, S can be neglected in the 10 nm I_{CNFET} equation without sacrificing accuracy.

ABSTRAK

Pengecilan nod teknologi transistor kesan medan separuh pengalir oksida logam (MOSFET) ke ukuran sub-nanometer menyebabkan kesan saluran pendek yang serius. Antara pelbagai teknologi dan struktur peranti yang telah dicadangkan, transistor kesan medan karbon nanotiub (CNFET) dikatakan calon yang paling sesuai untuk menggantikan MOSFET. Kesan parameter struktur terhadap prestasi litar penguat kendalian dua-peringkat adalah salah satu bidang penyelidikan yang aktif dalam mengkaji CNFET ketika pengecilan saiz daripada nod teknologi yang lebih besar ke nod teknologi yang lebih kecil. Penyelidikan ini mengkaji parameter struktur CNFET iaitu bilangan tiub (*N*), garis pusat karbon nanotiub (CNT) (D_{CNT}), dan jarak antara CNT (*S*) yang mengoptimumkan rekabentuk litar penguat kendalian dua-peringkat nod teknologi 32 nm dan 10 nm. Litar penguat kendalian ini dioptimumkan dengan penyimbangan gandaan gelung-buka, lebar jalur gandaan satu (UGB), pelesapan kuasa, dan rintangan keluaran untuk mendapatkan parameter struktur yang optimum. Litar penguat kendalian dua-peringkat optimum 10 nm kemudian dibandingkan dengan 32 nm untuk menilai parameter struktur optimum dan prestasi litar. Prestasi litar yang dinilai terdiri daripada gandaan gelung-buka, UGB, pelesapan kuasa, rintangan keluaran, julat ragam sepunya masukan (ICMR), nisbah penolakan ragam sepunya (CMRR), nisbah penolakan bekalan kuasa (PSRR), kadar slu, dan masa pengenapan. Selanjutnya, penyelidikan ini juga mengkaji kesan *S* terhadap arus saliran (I_{CNFET}) ketika beralih dari nod teknologi 32 nm ke 10 nm. Hasil simulasi menunjukkan bahawa reka bentuk litar 10 nm yang optimum telah berjaya meningkatkan prestasi litar lebih daripada 33% untuk semua metrik prestasi. Metrik prestasi yang paling banyak meningkat ialah UGB, peningkatannya sebanyak 109.99%. Siasatan terhadap kesan *S* kepada I_{CNFET} apabila saiz CNFET dikurangkan kepada nod teknologi 10 nm mencadangkan bahawa parameter *S* harus diambil kira dalam persamaan I_{CNFET} 32 nm untuk anggaran arus saliran yang tepat. Sebaliknya, untuk memudahkan pengiraan, *S* boleh diabaikan dalam persamaan I_{CNFET} 10 nm.

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LIST OF SYMBOLS AND ABBREVIATIONS

a	–	Lattice Constant of Graphene Sheet
A_V	–	Open-loop Gain
C_C	–	Compensation Capacitance
C_g	–	Gate Capacitance
C_h	–	Length of Chiral Vector
$\mathbf{C}_h$	–	Chiral Vector of SWCNT
C_L	–	Load Capacitance
D_{CNT}	–	CNT Diameter
e	–	Unit Electron Charge
E_g	–	Energy Bandgap
f_{3dB}	–	3 dB Bandwidth
f_T	–	Unity Gain Frequency
f_{UGB}	–	Unity-gain Bandwidth
g_{CNT}	–	Transconductance per CNT
g_m	–	Transconductance
g_{mN}	–	Transconductance of N^{th} CNFET
I_B	–	Bias Current
I_{CNFET}	–	CNFET Drain Current
I_{DS}	–	Drain-source Current
I_o	–	Current Source
I_{TUBE}	–	Current per Tube
L_{ch}	–	Channel Length
L_s	–	Source Length of the Doped CNT Region
N	–	Number of Carbon Nanotube
(n, m)	–	Chiral Index
R_L	–	Load Resistance
r_{oN}	–	Output Resistance of N^{th} CNFET

R_{out}	–	Output Resistance
R_X	–	Port Resistance X
R_Y	–	Port Resistance Y
R_Z	–	Port Resistance Z
S	–	CNT Pitch
SR	–	Slew Rate
$SR-$	–	Negative Slew Rate
$SR+$	–	Positive Slew Rate
V_{CM}	–	Common-mode Voltage Source
V_{DD}	–	Drain Voltage
V_{dd}	–	Drain AC Ripple
V_{DS}	–	Drain-source Voltage
V_{dsat}	–	Minimum Saturation Voltage
V_{GS}	–	Gate-source Voltage
$V_{GS, min}$	–	Minimum Gate-source Voltage
V_I	–	Differential Input Voltage
V_{in-}	–	Input Voltage Applied to the Inverting Terminal
V_{in+}	–	Input Voltage Applied to the Non-inverting Terminal
$V_{in, max}$	–	Maximum Input Voltage Range
$V_{in, min}$	–	Minimum Input Voltage Range
V_{OS}	–	Input-offset Voltage
V_{o1}	–	Output Voltage at a Particular Value of V_I without R_L
V_{o2}	–	Output Voltage at a Particular Value of V_I with R_L
V_{out}	–	Output Voltage from the High Gain Stage
V_{out}'	–	Output Voltage from the Buffer Stage
V_{SS}	–	Source Voltage
V_{ss}	–	Source AC Ripple
V_{th}	–	Threshold Voltage
V_π	–	Carbon π to π Bond Energy

W_{eff}	–	Effective Channel Width
W_g	–	CNFET Gate Width
α	–	Current Gain Value, Screening Effect Coefficient
β	–	Voltage Gain Value
θ	–	Chiral Angle
μ	–	Carrier Mobility
μ_n	–	Surface Mobility of N-channel CNFET
μ_p	–	Surface Mobility of P-channel CNFET
ρ_s	–	Source Resistance per Unit Length of the Doped CNT
ϕ_m	–	Phase Margin
1D	–	One-dimensional
3D	–	Three-dimensional
ADC	–	Analog-to-digital Converter
BJT	–	Bipolar Junction Transistor
BTB	–	Band-to-band
CCI	–	First-generation Current Conveyor
CCII	–	Second-generation Current Conveyor
CCII±	–	Dual-output Second-generation Current Conveyor
CCIII	–	Third-generation Current Conveyor
C-CNFET	–	Conventional CNFET
CMOS	–	Complementary Metal Oxide Semiconductor
CMRR	–	Common-mode Rejection Ratio
CNFET	–	Carbon Nanotube Field-effect Transistor
CNFET-FCOA	–	CNFET-based Folded Cascode Op-amp
CNT	–	Carbon Nanotube
CVD	–	Chemical Vapour Deposition
FET	–	Field-effect Transistor
FinFET	–	Fin Field-effect Transistor

GAAFET	–	Gate-all-around Field-effect Transistor
GBP	–	Gain-bandwidth Product
HSPUI	–	HSPICE User Interface
IC	–	Integrated Circuit
ICMR	–	Input Common-mode Range
IGFET	–	Insulated-gate Field-effect Transistor
IRDS	–	International Roadmap for Devices and Systems
ITRS	–	International Technology Roadmap for Semiconductors
MOSFET	–	Metal Oxide Semiconductor Field-effect Transistor
Mott FET	–	Mott Field-effect Transistor
MuGFET	–	Multi-gate MOSFET
MWCNT	–	Multi-wall Carbon Nanotube
NCNFET	–	N-channel CNFET
NEMS	–	Nanoelectromechanical Switches
NWFET	–	Nanowire Field-effect Transistor
op-amp	–	Operational Amplifier
OTA	–	Operational Transconductance Amplifier
PCNFET	–	P-channel CNFET
PSRR	–	Power-supply Rejection Ratio
$PSRR^-$	–	Negative PSRR
$PSRR^+$	–	Positive PSRR
QCA	–	Quantum-Dot Cellular Automata
SB-CNFET	–	Schottky Barrier CNFET
SET	–	Single-electron Transistors
SPICE	–	Simulation Program with Integrated Circuit Emphasis
SWCNT	–	Single-wall Carbon Nanotube
T-CNFET	–	Tunnelling CNFET
TFET	–	Tunnelling Field-effect Transistor

UGB – Unity-gain Bandwidth

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CHAPTER 1

INTRODUCTION

1.1 Background of study

In the early 20th century, an idea of controlling the flow of the electric current was proposed by a physicist and electrical engineer, Julius Edgar Lilienfeld [1]. He described the concepts of a new electronic device as well as owned the first patents on the proposed device in 1926 [2]. The device is known as the field-effect transistor (FET), which is widely used in integrated circuits (ICs) nowadays. After twenty-four years from the patent application, the bipolar junction transistor (BJT) proposed by William Shockley was first created [3]. The invention of BJTs initiated a new era in electronic, the transistor era. Meanwhile, the first type of transistor, the point-contact transistor developed by John Bardeen and Walter Brattain in 1947 was quickly replaced by the BJTs [3].

Due to the surface problems that existed in the bulk of the BJTs, M. M. Atalla et al., proposed a solution by introducing a new semiconductor device called the metal oxide semiconductor field-effect transistor (MOSFET) [4] and filed the patent in the following year [5], [6]. By comparing to the BJT, the MOSFET has the capability to be scaled down without dropping the performance. Scaling down MOSFET offers the improvement in speed and power dissipation. Concurrently, high performance computer can be achieved when more MOSFETs were scaled down and utilized. Hence, the existence of MOSFET triggered the rapid development of technology.

As the MOSFET has continuously been scaled, more transistors and devices can be packed and placed on a chip for a given area; thus, the chip with the smaller area has the same or more functionality. Besides, the scaling down of the MOSFET also contributed to the chip cost reduction. In the past decades, the shrinking trend of

transistors beyond the sub-10 nm technology node has become more and more significant. In 1975, Gordon Moore observed that the number of transistors per chip doubles in about every two years, known as Moore's Law [7]. The tendency of MOSFET scaling is due to the huge demand for decreasing the chip area as well as improving the performances of the transistors in terms of speed and power dissipation [8].

The MOSFET is the fundamental building block of the complementary metal oxide semiconductor (CMOS). CMOS is a technology that drives the advancement of today's electronic devices, from a simple calculator to the advanced supercomputer. For improving the performances of the CMOS, the scaling down is carried out year by year. However, the CMOS scaling has recently reached its limits because leakage drain current and short channel effect become more significant [8]. For this reason, several technologies and device structure variations have been proposed in the previous works such as the fin field-effect transistor (FinFET) [9], utilization of carbon nanotube (CNT) to form a structure called carbon nanotube field-effect transistor (CNFET) [10], quantum-dot cellular automata (QCA) [11], and single-electron transistor (SET) [12]. Among these devices, CNFET is the most promising candidate to replace the conventional MOSFET because of the similarities between the MOSFET and CNFET in terms of electrical properties as well as the fabrication process [13], [14].

1.2 Problem statement

MOSFETs dimension is continuously scaled down. The purpose of shrinking the dimensions of MOSFET devices is to reduce the area and power consumption while improving the operating speed and MOSFET density on the IC. Although the speed and density are increased, the downscaling limitations in MOSFET are becoming more significant when the dimension is scaled beyond 10 nm. The issues such as the short-channel effect, source to drain tunnelling, and the high electric field will cause the deterioration of device performances [15]. Hence, a CMOS extension device, CNFETs is seen to be a potential candidate for replacing the MOSFET as it has similar electrical properties and fabrication processes as MOSFET devices, but can be scaled beyond 10 nm without CMOS deficiencies [16]. Beside scalability, the CNFET has advantages in terms of ballistics transport, gain, gate-all-around, and ultra-thin body [17].

Recently, there are numerous published studies that describe the circuit designs using CNFET at 32 nm technology node [18]–[22]. A recent study by Waykole and Bendre provides the performance analysis of a two-stage operational amplifier (op-amp), designed by using the CMOS and CNFET at 32 nm technology [21]. The design parameters, number of carbon nanotubes (N), CNT diameter (D_{CNT}), and inter-CNT spacing, also called CNT pitch (S) were considered in the CNFET circuit design. The optimum values of CNFET design parameters were determined for obtaining the optimum circuit performances. The analysis and discussion were carried out by comparing the performances of CMOS and CNFET circuits.

From [21], two interesting questions can be asked as follows: (1) What are the optimum values of structural parameters for the two-stage op-amp design if we migrate from 32 nm to 10 nm technology node? and (2) Are the optimum parameter values for the 10 nm and 32 nm circuits the same? Therefore, the investigation of the optimum values of the structural parameters is essential to provide a reference about the influence of the structural parameters on the circuit performance when migrating to a smaller technology node. In this study, a two-stage op-amp with Miller compensation is selected as the circuit topology to be designed as the circuit has advantages in the performance parameters such as gain, output swing, noise, and bandwidth [23]. The two-stage op-amp with Miller compensation is one of the applications in high performance analog circuit. Furthermore, the investigation of the CNFET drain current (I_{CNFET}) is also conducted in this research because there is a relationship between I_{CNFET} and technology node, and I_{CNFET} is a major factor in CNFET circuit performance. Despite an approximated I_{CNFET} equation at 32 nm technology node was defined in the thesis from Jie Deng [24], the impact of S on I_{CNFET} at the 10 nm technology has yet to be studied. Several studies also provide no evidence for the inclusion of S in estimating I_{CNFET} in CNFET [13], [20], [25]. Thus, a deep exploration is indispensable to observe the effect of S on I_{CNFET} in 10 nm technology.

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APPENDIX E

LIST OF PUBLICATIONS

1. W. H. Chua, C. Uttraphan, and B. C. Kok, "An Optimum Design of the Carbon Nanotube Field Effect Transistor for Analog Applications in 10 nm Technology," in *2020 IEEE Student Conference on Research and Development (SCOReD)*, 2020, pp. 222–227, doi: 10.1109/scored50371.2020.9250982.
2. W. H. Chua, C. Uttraphan, "An Optimum Design of the Carbon Nanotube Field-effect Transistor for Analog Applications in 32 nm and 10 nm Technology", Accepted for publication to *Annals of Emerging Technologies in Computing* (*AETiC*). (Scopus)
3. W. H. Chua, C. Uttraphan, B. C Kok, N. Ahmad, "Performance evaluation of the two-stage CNFET operational amplifier at 32 nm and 10 nm technology nodes", Accepted for publication in: *Journal of Physics: Conference Series* (*JPCS*), Online ISSN: 1742-6596 and Print ISSN: 1742-6588. (Scopus & WoS)

APPENDIX F

VITA

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