DESIGNING MEMORY CELLS WITH A NOVEL APPROACHES BASED ON A NEW MULTIPLEXER IN QCA TECHNOLOGY

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ABSTRACT

Transistor-based CMOS technology has many drawbacks such that it cannot continue to follow the scaling of Moore's law in the near future. These drawbacks lead researchers to think about alternatives. Quantum-dot Cellular Automata (QCA) is a nanotechnology that has unique features in terms of size and power consumption. QCA has the ability to represent binary numbers by electrons configuration. The memory circuit is a very important part of the digital system. In QCA technology, there are many approaches presented to accomplish memory cells in both RAM and CAM types. CAM is a type of memory used in high-speed applications. In this thesis, novel approaches to design memory cells are proposed. The proposed approaches are based on a 2:1 multiplexer. Using the proposed approach of RAM cell, a singular form of RAM cell (SFRAMC) is accomplished. In QCA technology, researchers strive to design electronic circuits with an emphasis on minimizing important metrics such as cell count, area, delay, cost and power consumption. The SFRAMC demonstrated significant improvements, with a reduction cell count, occupied area and power consumption by 25%, 24% and 36%. In terms of implementation cost, the SFRAMC saves 43% of the cost when compared to the previous best design. On the other hand, by using the proposed approach of CAM cell, two different structures of the QCA-CAM cell have been introduced. The first proposed CAM cell (FPCAMC) gives improvements in terms of cell count, and delay by 15% and 17% respectively. The second proposed CAM cell (SPCAMC) gives improvements in terms of cell count, and delay by 6% and 17% respectively. In terms of total power consumption, both FPCAMC and SPCAMC have an improvement of about 53% over the best-reported design. The above features of the proposed memory cells (RAM and CAM) could pave the road for designing energy-efficient and cost-efficient memory circuits in the future.

ABSTRAK

Teknologi CMOS berasaskan transistor mempunyai banyak kelemahan yang tidak boleh terus mengikut skala undang-undang Moore dalam masa terdekat. Kelemahan ini menyebabkan penyelidik berfikir tentang alternatif lain. Quantum-dot Cellular Automata (QCA) ialah nanoteknologi yang mempunyai ciri unik dari segi saiz dan penggunaan kuasa. QCA mempunyai keupayaan untuk mewakili nombor binari dengan konfigurasi elektron. Litar memori adalah bahagian yang sangat penting dalam sistem digital. Dalam teknologi QCA, terdapat banyak pendekatan yang dibentangkan untuk mencapai sel memori dalam kedua-dua jenis RAM dan CAM. CAM ialah sejenis memori yang digunakan dalam aplikasi berkelajuan tinggi. Dalam tesis ini, pendekatan baru untuk mereka bentuk sel memori telah dicadangkan. Pendekatan yang dicadangkan adalah berdasarkan pemultipleks 2: 1. Menggunakan pendekatan sel RAM yang dicadangkan, bentuk sel tunggal RAM (SFRAMC) dicapai. Dalam teknologi QCA, penyelidik berusaha untuk mereka bentuk litar elektronik dengan penekanan pada meminimumkan metrik penting seperti kiraan sel, luas, kelewatan, kos dan penggunaan kuasa. SFRAMC menunjukkan peningkatan yang ketara, dengan pengurangan dalam bilangan sel, luas kawasan yang digunakan dan penggunaan kuasa masing-masing sebanyak 25%, 24% dan 36%. Dari segi kos pelaksanaan, SFRAMC menjimatkan 43% kos jika dibandingkan dengan reka bentuk terbaik sebelum ini. Cadangan menggunakan pendekatan sel CAM, dengan dua struktur sel QCA-CAM yang berbeza telah diperkenalkan. Cadangan sel CAM pertama (FPCAMC) memberikan peningkatan dari segi kiraan sel, dan kelewatan 15% dan 17%, masing-masing. Cadangan sel CAM kedua (SPCAMC) memberikan peningkatan dari segi kiraan sel, dan kelewatan 6% dan 17%, masing-masing. Sementara itu dari segi jumlah penggunaan kuasa, kedua-dua FCAMC dan SCAMC mempunyai peningkatan kira-kira 53% berbanding reka bentuk terbaik yang dilaporkan. Ciri-ciri di atas bagi sel memori yang dicadangkan (RAM dan CAM) boleh membuka jalan untuk mereka bentuk litar ingatan yang lebih cekap tenaga dan kos efektif pada masa hadapan.

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LIST OF SYMBOLS AND ABBREVIATIONS

CAM	–	Content Addressable Memory
CLB	–	Configurable Logic Block
CLF	–	Cells and Layout Factor
CMOS	–	Complementary Metal Oxide Semiconductor
CNT	–	Carbon Nanotube
DRAM	–	Dynamic RAM
E_{clock}	–	Clock signal Energy
E_i	–	Energy of the input cell
$E_{i,j}$	–	kink energy between the two cells i and j
E_k	–	Kink Energy
E_{net}	–	Net Energy
E_o	–	Output cell Energy
FET	–	Field-Effect Transistor
FPCAMC	–	First Proposed CAM Cell
FPGAs	–	Field Programmable Gate Arrays
GaAs	–	Gallium Arsenide
$\hbar$	–	Planck's Constant
Hi	–	Hamiltonian
KB	–	Boltzmann's constant
mev	–	Mille electron volt
MQCA	–	Molecular Quantum Cellular Automata
MUX	–	Multiplexer
Pi	–	polarisation of cell i
Pj	–	polarisation of cell j
PTM	–	Probabilistic Transfer Matrices
QCA	–	Quantum-dot Cellular Automata
Q-BART	–	Quantum Based Architecture Rules Tool

QCA-LG	–	QCA Layout Generator
RAM	–	Random Access Memory
RTD	–	Resonant Tunnelling Diodes
SCQCA	–	Split Current Quantum-dot Cellular Automata
SET	–	Single Electron Transistor
SFRAMC	–	Singular Form RAM Cell
SPCAMC	–	Second Proposed CAM Cell
SRAM	–	Static RAM
TCAM	–	Ternary CAM
Tr	–	Trace Operation
USMUX	–	Unique Structure of a 2:1 Multiplexer
VLSI	–	Very Large-Scale Integration
XOR	–	Exclusive OR gate
γ	–	Energy of electron tunnelling inside the cell
Γ	–	Energy environment of the cell
λ	–	Coherence vector
λ_{ss}	–	Steady-state coherence vector
P	–	Density matrix
σx, σy and σz	–	Pauli spin matrices
τ	–	The time of relaxation

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CHAPTER 1

INTRODUCTION

1.1 Introduction

The current century trend is information, so information storage became an essential issue. High speed, low power consumption and efficient data storing circuits are among the major challenges in information technology.

Transistor-based CMOS technology has many drawbacks such as power consumption and soon cannot continue to follow Moore's law and system scaling on a chip. These drawbacks lead the researchers to think about alternative technologies. Emerging nanotechnology can overcome the scaling limitation in the current CMOS technology; some of these techniques are Single Electron Transistor (SET), Resonant Tunnelling Diodes (RTD), Carbon Nanotube (CNT) and Quantum-dot Cellular Automata (QCA). Among these evolving nanotechnologies, QCA uses the new paradigm for computation and it is promising in terms of power consumption [1, 2]. The device density in QCA is about 10^{12} devices/cm^2 and the speed operating in THz [3]. QCA is capable of implementing logical functionality by controlling the position of electrons.

The unique features of QCA technology in terms of power consumption, size and speed have made it the focus of researchers, especially those interested in digital circuits. improving the memory circuit is an important issue as the core of the digital world. So, the main contribution of this thesis is to design optimal QCA-architectures of memory cells by suggesting new design approaches.

1.2 Motivation

Although the era IC technology created by CMOS in the VLSI domain with an optimised form of digital circuits, it has some limitations to continue integrating with nanoscale devices such as expensive lithography, short channel effects, doping fluctuation, and power dissipation [4]. The researchers were looking for a new nanotechnology to be a good solution to replace CMOS technology.

QCA technology uses a new physical phenomenon where it replaces the voltage level for digital representation with the cell configuration [5]. The main building blocks in the QCA circuit are majority gate and inverter, where the majority gate can configure AND/OR gates. In this case, the circuit can be constructed with only majority and inverter blocks by following Boolean functions. Adopting the classical logical designs used for CMOS to the QCA technology produces non-optimal circuits, especially in memory design [6-10].

QCA has inherent capabilities where logic circuits can be designed using the intercellular effects without following any Boolean functions [11]. This feature was recently discovered and there are several attempts to build logic gates using it. Since this feature is of importance in improving the QCA circuits in terms of area, number of cells, dissipated power and latency, so it gave us the impetus to build memory cells in this thesis. The current memory cells in the QCA literature are presented in different approaches aiming to minimise the power, area, complexity and cost. In this work, these methods will be studied and compared to determine a starting point that ends with the design of different structures of memory cells.

1.3 Objectives

1- To design a low-complexity 2:1 multiplexer based on the intercellular effects as inherent capability of QCA technology.
2- To find out a new designing approaches of QCA-RAM cell and QCA-CAM cell based on the proposed multiplexer.
3- To construct QCA forms of memory cells based on the proposed multiplexer and using the proposed approaches.

1.4 Contributions

This thesis provides an overview of digital representation using QCA technology. QCA technology is one of the candidate technologies to be an alternative to CMOS technology. QCA has many features that cannot be found in other technology in that it does not require any power source except the clock circuit that performs the synchronisation and determines the direction of data flow. The main gate in QCA circuits is majority gate where it used to perform AND and OR gates. Any Boolean equation can be represented in QCA technology with only majority gate and inverter. In addition to what has been mentioned, QCA technology has inherent properties so that it is possible to design QCA circuits without need to follow Boolean equations. This feature has not been sufficiently exploited, so researchers are still exploring several logic gates that save area, delay, and cost. In this thesis and after focusing on this feature, the main contributions are described in the following:

1- A new QCA-structure of the 2:1 multiplexer (USMUX).
2- A novel approach for designing RAM cell.
3- A new QCA structure of RAM cell based on the proposed approach and utilising the USMUX.
4- A novel approach for designing CAM cell.
5- Two different structures of QCA-CAM cell follow the proposed approach and utilising the USMUX.

1.5 Scope

In this thesis, the circuit's simulation will be the method to design the proposed circuits because it is challenging to implement QCA circuits until now. The simulation result is currently limited by the clock scheme supported by the designer software. In this work, the QCADesigner tool [12] used as a simulation software to show the operational behaviour of the circuits and the input-output graphs. This tool is built based on the coherence and bi-stable mathematical models. Furthermore, another application called QCAPro is used in this thesis to calculate the energy consumption.

CHAPTER 2

PRELIMINARIES AND RELATED WORK

2.1 Introduction

In recent years, the researchers paid attention to the emerging nanotechnology to bypass the CMOS limitations. Quantum-dot Cellular Automata is a transistor-less technology can represent binary numbers in new paradigm where it did not required flow of current. This chapter begins with a background of QCA technology before moving on to modelling. The concept of QCA is quite simple, the basic unit can be modelled as a bistable system that is controlled by a clock signal. Different methods have been introduced to physically demonstrate this concept but it is still under development as will summarised in this chapter. Like other techniques, there are different challenges in QCA technology under investigation which will also be highlighted. Finally, related work will be reviewed in the last three sections.

2.2 Technology Background

QCA was invented in 1993 by Lent et al. [13]. The main element in QCA is a square cell containing four dots and two electrons. The Coulomb interaction forces electrons to occupy the dots in antipodal sides. For binary computation, CMOS uses voltage levels whereas QCA uses the location of electrons inside the cell. Cell polarisation represents logic “0” or logic “1”, where each cell will have the opportunity to have two different polarisations, depending on the location of electrons. Switching states are carried out by allowing the particles to tunnel between the dots mechanically. The

tunnel junction is illustrated in Figure 2.1 (a). The two types of QCA cells are shown in Figure 2.1 (b). Due to the Coulomb interaction, the information will exchange with the adjacent cells. The input cell will drive the neighbouring cell to be in the same polarisation. So, it forces the input cell to a specific polarisation that is only required. If many cells are put beside each other, a QCA binary wire will be constructed. Figure 2.1 (c) shows the propagate information of neighbouring cells across a wire [14].

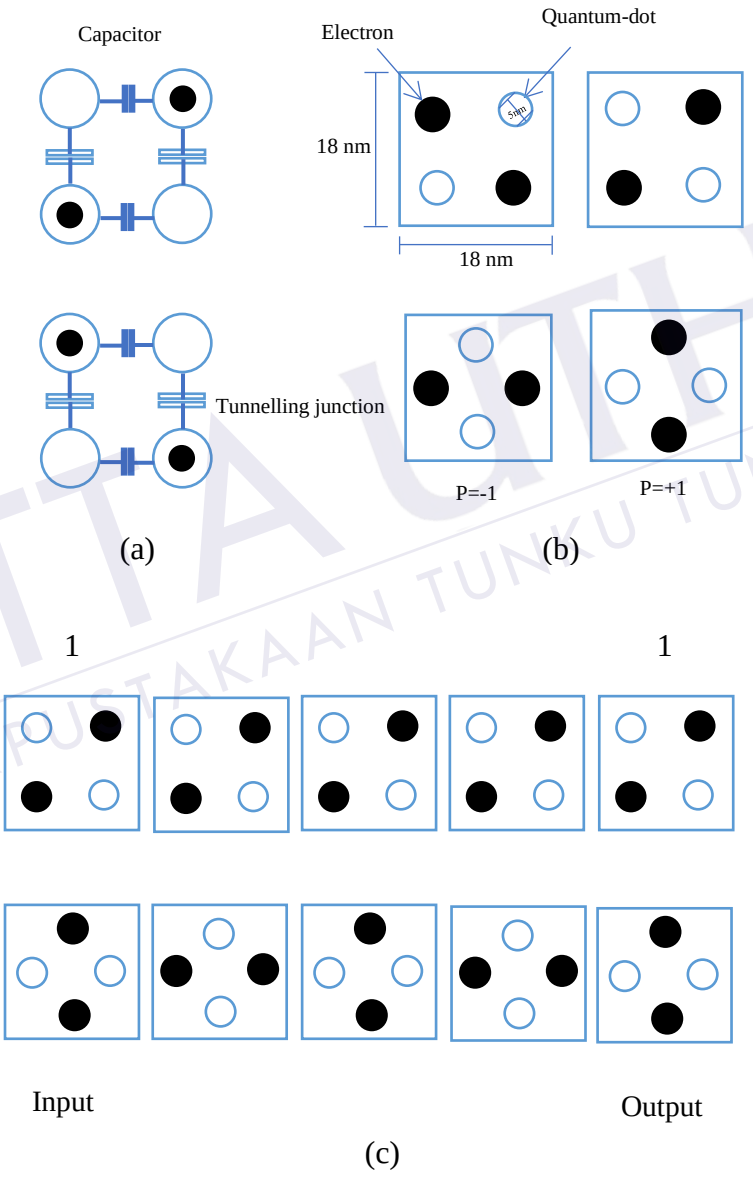


Figure 2.1: QCA cells (a) Functional outline, (b) types, (c) wires

To find out the polarisation of a cell, the dots are numbered starting from the upper dot on the right side and in a clockwise direction, as shown in the Figure 2.2. A cell's polarisation is determined by equation 2.1.

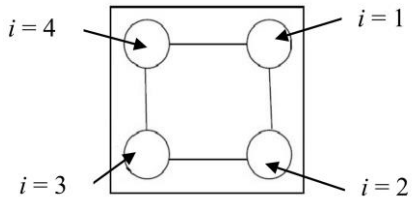


Figure 2.2: Unpolarised QCA cell

$$P = \frac{(\mathcal{P}1+\mathcal{P}3)-(\mathcal{P}2+\mathcal{P}4)}{\mathcal{P}1+\mathcal{P}2+\mathcal{P}3+\mathcal{P}4} \quad (2:1)$$

where, $\mathcal{P}$ represents the presence of the electron inside a dot i, i=1 if the dot has an electron and 0 if the dot is empty. So that if dots 1 and 3 have electrons, the polarisation of the cell (P) equals +1 otherwise if dots 2 and 4 have electrons, then P equals -1.

2.2.1 Clocking

Data is controlled by the clock signal and represented by the polarisation of cells [15]. The clock signal is commonly generated by CMOS wires buried under the QCA circuitry [3]. Thus, many reasons make clocking very essential to apply in QCA circuits:

(a) Control the flow of information: The flow of information from the input to the output cell can be controlled by a clock signal in QCA because there is no current flow in this Nano-technique.

(b) It constrains the circuit to remain in the quantum mechanical ground state, an essential condition to accomplish QCA duly working.

(c) Timing control: For controlling the timing of the QCA circuits, the clock signal should be used as it is the only tool to do this, in addition to ensuring quick switching and quick relaxation, as the clocked cells relax faster than non-clocked.

(d) It creates pipelines if utilised multiple clock signals: To prevent the KINK state which happens when a huge number of cells are switched together. May stumble into the minimum local energy and cannot reach the ground state. The QCA circuit is split up into multiple specific zones clocked with multiple clock signals. This handles the issue of the KINK state and gives pipelining for QCA systems.

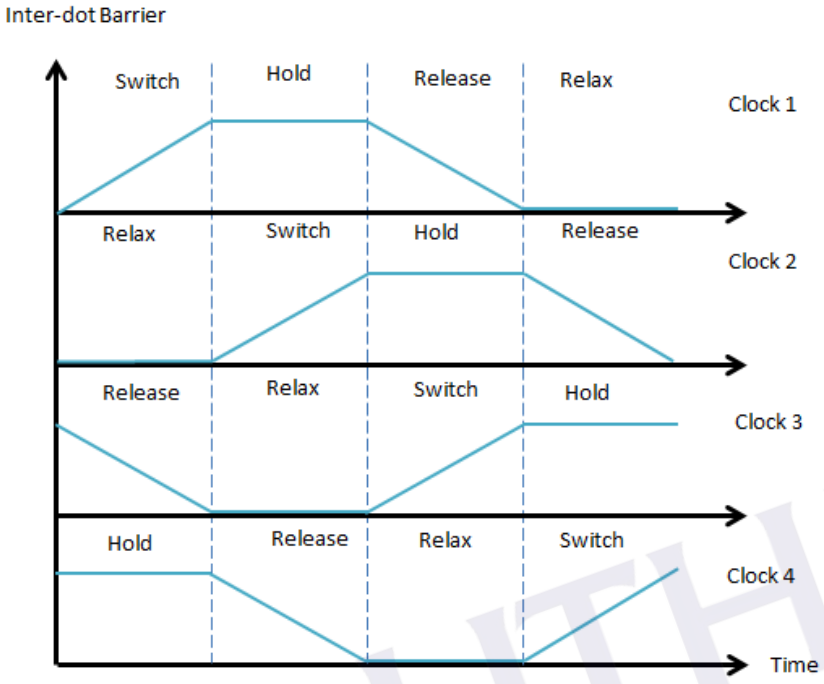
(e) To revive the lost signal energy to the environment: for one clock cycle, the net energy in the QCA system could be expressed as equation 2.2**.**

$$\boldsymbol{E_{net} = E_i + E_{clock} - E_{diss} - E_o} \tag{2.2}$$

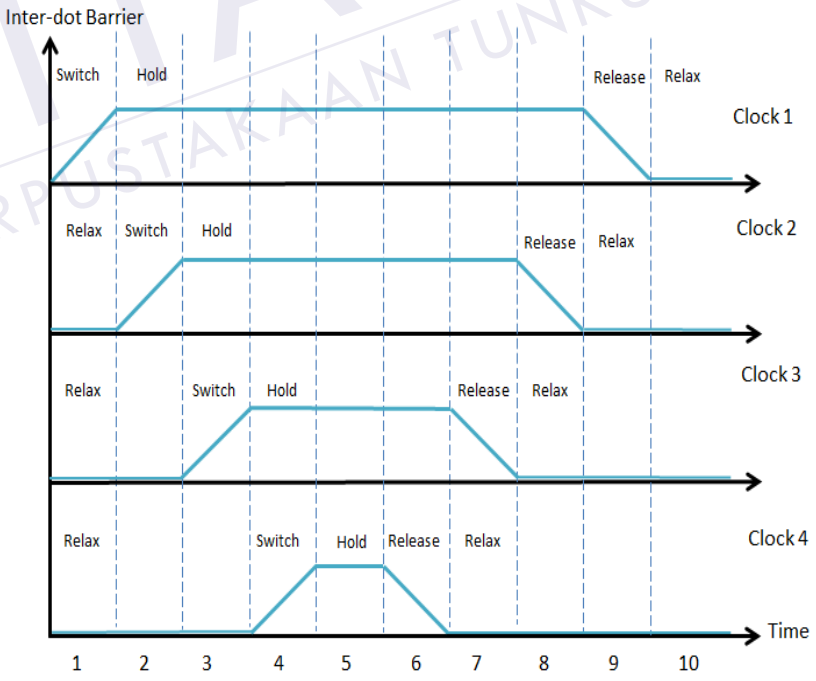
where E_{net} is the net energy change, E_i is the energy of the driver (input cell), E_o is the consumed energy by the output cell, E_{diss} is the dissipated energy along the signal path. So, E_{clock} is essential to compensate for the energy loss in the path to ensure a net energy change of zero.

Generally, the clock in the QCA circuit has four states to provide an adiabatic switching state and not abrupt. This is because in abrupt switching the input is suddenly changed to the QCA circuit. As a result, the circuit is exciting and will relax the ground state by dissipating energy to the environment. Therefore, relaxation will be inflexible and uncontrollable, where the circuit may enter a stable state that can be determined by a local, rather than a global, ground state. On the other hand, in adiabatic switching, the relaxation is manipulated by the switch phase and release phase, so the circuit is always in its ground state. There are two types, commonly used, as clocking signals in the QCA circuits, the first one is Landauer [16] as shown in Figure 2.3 (a) and the second type is Bennett clock [17] as shown in Figure 2.3 (b). The Bennett clock support reversable operation to reduce the power dissipation but the system speed is the impacted negatively. The clock signals in QCA are generated by an electric field, supplied by either Carbon Nanotubes (CNTs) or CMOS burned below the QCA circuit, applied to cells either to raise the tunnelling barrier or to lower it. When the barriers are low, the cells are unpolarised. In this state, electrons are free to change their location. If the barrier goes up, the electron tunnelling ratio will decrease. If the barriers reach maximum, the electrons cannot escape their dots in this state. Adiabatic switching is accomplished by reducing the barrier, evacuating the past input, applying

the present input and after that raising the barrier. If transitions occur sequentially, the system will remain near the ground state [14].



(a)



(b)

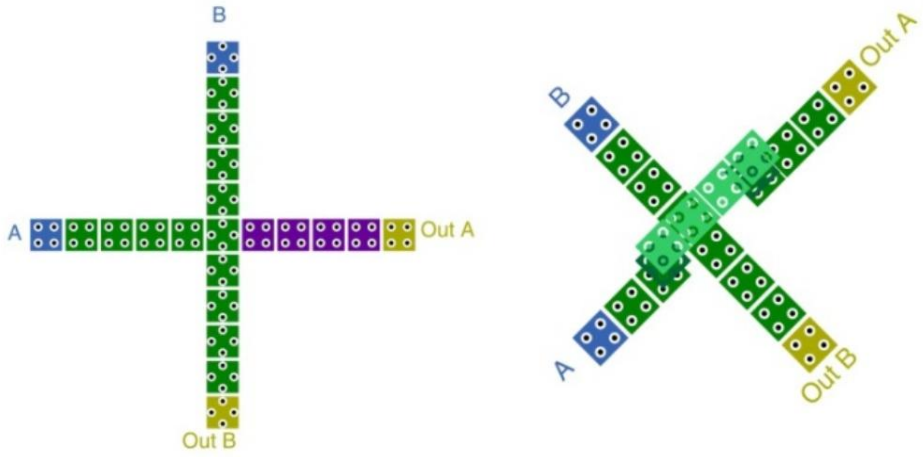
Figure 2.3: Clock signal proposed by (a) Landauer [16] and (b) Bennett [17]

2.2.2 Wire crossing

The problem of component interconnection or wire crossing in QCA technology must be solved to go ahead to be a suitable replacement for the current IC in fabrication. There are three strategies were proposed up to now to handle wire crossing in QCA, which are:

(a) Coplanar crossing: This strategy is accomplished using two types of QCA cells; these two types of wires are perpendicular to each other. One of these wires has cells in the rotating form, and the other wire uses non-rotating or direct cells. Thus, they can work independently and cross in the same layer, as illustrated in Figure 2.4 (a). However, this type of crossing can be easily affected by manufacturing defects, which is the biggest drawback. Therefore, if any cell deviates (misaligned) from its position, it will result in a cross-coupling between the operations of two wires. To increase the robustness of this type of wire crossing, many research has been done such as in [18, 19] but most of them lead to a significant increase in overhead.

(b) Multi-layer wire crossing: This strategy needs to implement multiple active QCA layers on top of each other, making it difficult for implementation. The crossing will be done in this method in another layer, as shown in Figure 2.4 (b). The same cell types can be used as long as the vertical distance between wires is sufficient to prevent signals from leaking from one layer to another, and there is a way to create cells stacked between layers.



(a) (b)

Figure 2.4: wire crossing (a) Coplanar; (b) multi-layer

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APPENDIX A

LIST OF PUBLICATIONS

Papers Extracted from Thesis

[1] M. Ali Hussien, Z. Mohd Shamian, and A. Esam, "Quantum-dot Cellular Automata: Review Paper," International Journal of Integrated Engineering, vol. 11, 12/30 2019.

[2] Majeed, A.H., Alkaldy, E., Zainal, M.S., Navi, K. and Nor, D. (2020), "Optimal design of RAM cell using novel 2:1 multiplexer in QCA technology", Circuit World, Vol. 46 No. 2, pp. 147-158

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[4] A. H. Majeed, A. Abdulelah, M. S. Zainal, and E. Alkaldy, "Design of Power-Efficient Structures of the CAM Cell using a New Approach in QCA Nanoelectronics Technology," Indonesian Journal of Electrical Engineering and Informatics (IJEEI), vol. 9, 2021.

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[1] Ali H. Majeed, E. AlKaldy, MSB Zainal, and Danial BMD Nor, "A new 5-input Majority Gate Without Adjacent Inputs Crosstalk Effect in QCA Technology," Indonesian Journal of Electrical Engineering and Computer Science, vol. 14, pp. 1159-1164, 2019

[2] A. H. Majeed, B. Salih, M. S. bin Zainal, and D. Bin Md Nor, "Power Efficient Optimal Structure CAM-Cell in QCA Technology," Indian Journal of Science and Technology, vol. 12, 2019.

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