CHAPTER 10

THE FAILURE OF INTEGRATED CIRCUIT: TEST AND ANALYSIS

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ABSTRACT

Failure analysis (FA) is an important function in the development and manufacturing of integrated circuits. It provides essential information for troubleshooting a complex device while ensuring reliability of a product. The objective of FA is to identify cause of failure and initiate corrective actions. Complex engineering knowledge is required in understanding the nature of a device failure, identifying the problem and subsequently providing a solution to avoid the failure again during the production of the device. FA identifies the causes of failure by analyzing stresses and other mechanisms causing failure. Device failure is defined as any non-conformance of the device to its electrical and/or visual/mechanical specifications. A failure mechanism usually leads to an identifiable change in a device. This chapter reveals the common techniques in troubleshooting IC and flow for identifying FA which consists of fault localization, de-processing, defect localization and inspection characterization. A failed component can provide important information to enhance the reliability of a device or product.

Keywords: failure analysis, troubleshooting, fault localization, reliability

10.1 INTRODUCTION

Current manufacturing is driven by the rapid technological changes. High technology manufacturing processes are increasingly moving towards flexible, intelligent production systems [1]. It is now a common
manufacturing practice to reduce and minimize the number of defects and errors in a process and to do things right at the first time. The ultimate aim is to reduce the number of defected products to zero. However, zero-defect means zero failures during operation but not necessarily implies zero imperfections, blemishes, or nonconformities [2].

Failure Analysis (FA) is the process of determining the physical root cause of component failure, troubleshooting a device, where determining how or why a semiconductor device has failed. Failure analysis is necessary in order to understand what caused the failure and how it can be prevented in the future. Device failure is defined as any non-conformance of the device to its electrical and/or visual/mechanical specifications. Therefore, destructive and non-destructive methods involved during the analysis process. Sometimes non-destructive analysis can turn into destructive analysis due to improper handling and incorrect technique performed on the sample.

### 10.2 Failure Analysis Terminology

Some terminology associated with failure analysis will be introduced. These terms are commonly used in written report and communications between the failure analysis department and the customers. The customer plays the key role in specifying the specifications of a device explicitly. The terms are as presented in Table 1.

<table>
<thead>
<tr>
<th><strong>Failure Description</strong></th>
<th><strong>Statement that explains on device failure; normally how much the device deviating from the specifications stated.</strong></th>
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<tr>
<td><strong>Failure Mechanism</strong></td>
<td><strong>Detailed description on the anomalies behind the failure of a device.</strong></td>
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<td><strong>Root Cause</strong></td>
<td><strong>Cause or factor a nonconformance and the fundamental reason for the occurrence of a problem.</strong></td>
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<tr>
<td><strong>Fault Localization</strong></td>
<td><strong>Step to localize and narrow down the area of failed part and isolate the defective areas.</strong></td>
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Table 1: Terminology used in failure analysis
10.3 FAILURE ANALYSIS PROCESS FLOW

Failure analysis starts with failure verification. Failures can occur during several points of a product’s life cycle and during manufacturing. It is important to validate the failure of a sample prior to failure analysis in order to conserve valuable FA resources. Failure verification is usually performed to characterize the failure mode. Moreover, good characterization of the failure mode is necessary to make the FA efficient and accurate.

After failure verification, the failure analysis engineer subjects the sample to various FA techniques step by step, collecting attributes and other observations along the way. Attributes is referred to properties, characteristics and functionality of the samples in order to find the root cause of the failure. Failure analysis start with non-destructive analysis and if necessary destructive analysis will be performed subsequently. The results of various steps must be corroborative and consistent. Any inconsistency in results must be evaluated before proceeding to the next FA step. The most important factor in failure analysis is how far the failure location can be narrowed down while still maintaining the failure symptoms (undestroyed state).

10.4 NON-DESTRUCTIVE ANALYSIS

For failure analysis, non-destructive test will be first considered before proceeding with the destructive test. Non-destructive test is challenging in preserving the actual failure at localized spot and it involves with tedious process [3]. Non-destructive techniques are those the steps that do not involve and cause any permanent change to the device. Figure 1 shows the general process flow in failure analysis.
Figure 1: The basic failure analysis flow

In order to understand the failure from customer’s, verifications step are very important. During verifications, samples must be in same condition as in return by customers. During verifications step, normally destructive test not allowed to do in the samples. As in Table 2, non-destructive tests are listed with the function of each test.
### Table 2: Non-destructive technique and purpose

<table>
<thead>
<tr>
<th>Technique</th>
<th>Purpose and Application</th>
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<tr>
<td>Failure Verification</td>
<td>Process of validating the failure of the sample. The best way to verify a failure is to electrically test the samples using the automatic test equipment (ATE) used during production testing. For simple test such as for short or open test, bench testing and current-voltage (I/V) curve tracing are very good techniques. They are fast for complementing ATE testing for failure verification and characterization.</td>
</tr>
<tr>
<td>Optical Microscopy</td>
<td>To inspect any anomalies on external or internal samples.</td>
</tr>
<tr>
<td>X-ray Radiography</td>
<td>To examine the interior details of the samples without open the samples.</td>
</tr>
<tr>
<td>Curve Tracing</td>
<td>To check the current-voltage characteristics of an electrical path.</td>
</tr>
<tr>
<td>Scanning Acoustic Microscopy (SAM)</td>
<td>To detect delamination or disbond between package interfaces, e.g., interfaces between the plastic resin package material, the die, the die paddle, the lead-frame, the die attach material, etc.</td>
</tr>
</tbody>
</table>

10.5 **DESTRUCTIVE ANALYSIS**

After a failure is confirmed (during non-destructive), the next part is localized the area of failure. In this step, normally the will open for visual inspection and other steps in the internal package. In destructive techniques, the samples will change and alter permanently either by using chemical, mechanical or electrical methods [4-5]. Table 3 list steps that call as destructive techniques and the applications.

10.6 **FAULT LOCALIZATION**

Fault localization is a technique to locate faults or failure in a sample. This process is not fixed to one technique only, but it involves with many techniques in order to define the root cause of the failure [6]. Both software and hardware diagnostics tools will be used in this process. The size and
complexity of an electronic devices challenging factors to accurately localize faults prior to any destructive FA tests. Normally, destructive technique such as photon emission microscopy (PEM), fluorescent micro-thermal imaging and liquid crystal hot spot analysis are used to localize the failure areas [7].

These tools are expensive and require experienced personnel trained in integrated circuit (IC) layout, testing and the technique itself in order to optimize the testing processes. Both of physical and electrical steps are required to identify and localize the failure. In modern devices, fault localization step is more challenging due to complexity of the package and complexity of the systems in the devices increased sharply. The complexity is defined as the total number of transistors and the total wiring length on the IC.

Table 3: Destructive test techniques and applications

<table>
<thead>
<tr>
<th>Technique</th>
<th>Application</th>
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<tr>
<td>Decapsulation</td>
<td>A process for opening the IC package before visual inspection, chemical analysis, or electrical examination of the die and the internal features of the package. For hermetic package, the process is referred to as 'delidding' or 'decapping.'</td>
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<tr>
<td>Cross Sectioning</td>
<td>A technique for mechanically exposing a plane of interest in a die or package for further analysis or inspection. Normally, this consists of sawing, grinding, polishing, and staining the specimen until the plane of interest is ready for optical or electron microscopy</td>
</tr>
<tr>
<td>Hot Spot Detection/Liquid Crystal</td>
<td>To locate areas on the die surface that exhibit excessive heating. Excessive heating indicates a high current flow, which may be due to die defects or abnormalities like dielectric ruptures, metallization shorts, and leaky junctions.</td>
</tr>
<tr>
<td>Light Emitting Microscope</td>
<td>A technique for detection of light-emitting defects</td>
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</table>
Microprobing

To achieve electrical contact with or access to a point in the active circuitry of the die. Electrical contact is made by dropping fine-tipped probe needles directly on the point of interest, or on an area to which the point of interest is connected.

Scanning Electron Microscope (SEM)

For inspecting topographies of specimens at very high magnifications with real-time imaging.

Energy Dispersive X-ray (EDX)

For identifying the elemental composition of the specimen, or an area of interest.

Figure 2: Electrical over-stress phenomena. (a) Bulging of package, (b) Burnt or crack package, (c) Burnt Metal and (d) heat stressed silicon.
10.7 ROOT CAUSES IN IC FAILURES

After localizing the area of failure in an integrated circuit, failure analysis engineer will find the cause of the failure. Anomalies in the function of the sample is caused by the change of resistance in between any electrical nodes or in any electrical path of the samples. However, the samples normally do not fail for electrical reasons but caused by either physical, chemical, or mechanical faults.

The two main classifications of failures are overstress and wear-out. Overstress is a condition where extreme conditions were applied exceeding the strength of materials. The condition occurs abruptly, and it is catastrophic [8]. Wear-out is an accumulation of damage under extended usage or repeated stress applications. Wear-out and overstress test can be detected as early during reliability test.

The major failures are due to electrical overstress (EOS) and electrostatic static discharge damage (ESD). EOS phenomena are the thermal damage that occur when the device is subjected to a voltage and current that induced heat which is over the specified heat limits of the device [9-10]. Heat generated during EOS event result of resistive heating and localized high temperatures in the devices. Some examples are as shown in Figure 2. The high temperature causes destructive damage to the materials used in the device’s construction.

Electrostatic Discharge (ESD) is a phenomenon when abrupt current flows between two electrically charged objects caused by contacts, an electrical short, or dielectric breakdown. ESD can create electric sparks and causes two main failures. First failure is associated with the danger of gate oxide dielectric breakdown due to the high voltage seen during ESD events in a CMOS device [11]. The thin gates of an input buffer are tied directly to the input pin and thus, are especially vulnerable to oxide breakdown. Dielectric breakdown is also of concern within the protection circuits since thin-gate MOS devices are commonly used.

The second effect from ESD stress is melting of material due to Joule heating which refers to the resistive heat generated by a current moving through an electric field. If the high current of an ESD event produce high current which is sufficiently localized in an area of high electric field, second breakdown would occur. This is leading to either device failure, i.e., shorts and opens, or the substantial damages under increased leakage current.
This chapter summarizes general steps in failure analysis. Failure analysis and investigation are to determine the root cause of failure the devices, component or asset fail or not perform as expected. The findings from failure analysis will be used to take remedial action and prevent from recurrence.

REFERENCES


