SINGLE-SWITCH BRIDGELESS PFC SEPIC WITH PROPOSED SERIES-LINE-DIODE-CLAMPED CONFIGURATION FOR DATA COMMUNICATION APPLICATIONS

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A thesis submitted in fulfillment of the requirement for the award of the Degree of Master of Electrical Engineering

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Special dedicated to

My beloved father,
Romai Noor Bin Yaacob

My beloved mother,
Esah Binti Abd Wahab

and

My family, supervisor, co-supervisors, lecturers and friends who have encouraged, guided and inspired me throughout this journey of education.
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In the name of Allah, the Most Beneficent and Most Merciful.

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ABSTRACT

This research presents a Single-Switch Bridgeless PFC (SSBPFC) SEPIC which is passive PFC with proposed series-line-diodes-clamped (SLDC) configuration for circuit structure simplicity and power quality issues mitigation. The structure simplification considers the reduction in number of components, while the power quality issues considers the parameters design of components. Basically, the BPFC SEPIC consists of more number of components and has the possibility of having power quality issues due to the combination of two operation circuits in one converter. When the BPFC SEPIC was implemented, several major drawbacks exist such as circulating current, capacitive coupling loop, more current stress at input capacitors and line-diodes, high total harmonic distortion of current (THDi), low power factor, dead zones, and high output voltage ripple. Therefore, a SSBPFC SEPIC structure with SLDC configuration was presented to solve the major drawbacks of the previous BPFC SEPIC. The principle employed for optimisation of parameters design was based on the energy balancing compensation between the input capacitors and output inductors to reduce the THDi. Besides, the input and output inductors were designed to operate in DCM and CCM respectively based on the ripple balancing concept to improve the quality of AC source. A large value of output capacitor was used to reduce the output voltage ripple. The simulation and experimental results showed a good agreement with the proposed designed parameters. The experimental results demonstrated that the THDi was reduced from 56.2% to 4.7% after optimisation and the dead zones were inherently eliminated. It was confirmed that the output voltage ripple frequency was always double from the line frequency, 50 Hz and the output voltage ripple was reduced from 19 V to 7 V and consequently produced a constant DC output voltage. The circulating current and capacitive coupling loop were eliminated, causing the maximum current stress at line-diodes and input capacitor to be reduced. Therefore, the design of the proposed converter was confirmed with approximately 100 W of the output power.
ABSTRAK

CONTENTS

TITLE i
DECLARATION ii
DEDICATION iii
ACKNOWLEDGEMENT iv
ABSTRACT v
ABSTRAK vi
CONTENTS vii
LIST OF TABLES xiv
LIST OF FIGURES xv
LIST OF SYMBOLS AND ABBREVIATIONS xx
LIST OF APPENDICES xxii

CHAPTER 1 INTRODUCTION 1
1.1 Project background 1
1.2 Problem statements 3
1.3 Objectives of research 4
1.4 Scope of research 5
1.5 General research framework 5
1.6 Thesis outline 7

CHAPTER 2 A REVIEW ON REDUCTION IN NUMBER OF POWER CONVERTERS AND POWER QUALITY ISSUES RELATED TO DATACOM APPLICATION 8
2.1 Overview 8
2.2 Datacom and Telecom applications based on power conversion issues 9
   2.2.1 Brief history of Nippon Telegraph and Telephone (NNT) for future goals 9
2.2.2 Improvement of AC system to DC system for Datacom and Telecom applications 10
2.2.3 Basic configuration and standards of Datacom and Telecom applications 11
2.2.4 Different polarity of input for Datacom and Telecom applications 12

2.3 Significance of power converter in Datacom application 14
2.3.1 Types of AC-DC converters 14
2.3.2 Types of DC-DC converters 15
2.3.3 Integration of full-bridge rectifier and SEPIC structures 16

2.4 Circuit structures compactness consideration of converters in Datacom application 17
2.4.1 Family of BPFC topologies 18
2.4.2 General classification of PFC circuits 21
2.4.3 Major issues on BPFC SEPI C circuit structures 22

2.5 Power quality issues of power converters 23
2.5.1 Harmonic distortion and total harmonic distortion 23
2.5.2 Power factor and power factor correction 24
2.5.3 Waveform distortion 25
2.5.4 Output voltage ripple 26

2.6 Research gap 27

CHAPTER 3 IMPROVEMENT OF BPFC SEPIC STRUCTURES TO REDUCE NUMBER OF PASSIVE COMPONENTS 28
3.1 Overview 28
3.2 Parameters consideration of passive components for improvement of structures 29
<table>
<thead>
<tr>
<th>Section</th>
<th>Title</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>3.3</td>
<td>Issues in separated-operation and shared-operation structures</td>
<td>30</td>
</tr>
<tr>
<td>3.4</td>
<td>Improvement of separated-operation structures for circulating current elimination</td>
<td>31</td>
</tr>
<tr>
<td></td>
<td>3.4.1 Two-switch BPFC SEPIC structure</td>
<td>32</td>
</tr>
<tr>
<td></td>
<td>3.4.2 Single-switch BPFC SEPIC structure</td>
<td>34</td>
</tr>
<tr>
<td>3.5</td>
<td>Improvement of shared-operation structures by reducing number of components</td>
<td>36</td>
</tr>
<tr>
<td></td>
<td>3.5.1 Two-switch BPFC SEPIC structure</td>
<td>37</td>
</tr>
<tr>
<td></td>
<td>3.5.2 Single-switch BPFC SEPIC structure</td>
<td>38</td>
</tr>
<tr>
<td>3.6</td>
<td>Optimisation of shared-operation structure for elimination of circulating current, capacitive coupling loop and reduction of number of components</td>
<td>39</td>
</tr>
<tr>
<td></td>
<td>3.6.1 SLDC as the improvement of proposed configuration</td>
<td>40</td>
</tr>
<tr>
<td></td>
<td>3.6.2 SSBPFC SEPIC structure with SLDC configuration</td>
<td>40</td>
</tr>
<tr>
<td>3.7</td>
<td>Analysis and parameters design for SSBPFC with SLDC configuration</td>
<td>43</td>
</tr>
<tr>
<td></td>
<td>3.7.1 Voltage conversion ratio, ( M )</td>
<td>44</td>
</tr>
<tr>
<td></td>
<td>3.7.2 Gain ratio as function of duty cycle, ( D )</td>
<td>45</td>
</tr>
<tr>
<td></td>
<td>3.7.3 Design of input inductors, ( L_1 ) and ( L_2 )</td>
<td>45</td>
</tr>
<tr>
<td></td>
<td>3.7.4 Boundaries between CCM and DCM</td>
<td>46</td>
</tr>
<tr>
<td></td>
<td>3.7.5 Design of output inductor, ( L_o )</td>
<td>47</td>
</tr>
<tr>
<td></td>
<td>3.7.6 Design of input capacitor, ( C_I )</td>
<td>47</td>
</tr>
<tr>
<td></td>
<td>3.7.7 Design of output capacitor, ( C_o )</td>
<td>48</td>
</tr>
<tr>
<td>3.8</td>
<td>Designs consideration for parameters design observation</td>
<td>48</td>
</tr>
</tbody>
</table>
3.8.1 Design 1: AC voltage source of 230 V and output power of 200 W

3.8.2 Design 2: AC voltage source of 50 V and output power of 100 W

3.9 Summary

CHAPTER 4 OPTIMISATION OF PASSIVE COMPONENTS PARAMETERS TO MITIGATE POWER QUALITY ISSUES

4.1 Overview

4.2 Principle of full-bridge diodes rectifier and BPFC with SLDC configuration for output characteristics

4.2.1 Full-bridge diode rectifier with inconstant DC output

4.2.2 BPFC with SLDC configuration structure with chopped DC output

4.2.3 Output voltage gain versus duty cycle based on SLDC configuration

4.3 Behaviour of conventional PFC SEPIC and BPFC SEPIC, and SSBPFC SEPIC with SLDC configuration

4.3.1 Conventional PFC SEPIC structure

4.3.2 Conventional BPFC SEPIC structure

4.3.3 SSBPFC SEPIC structure with SLDC configuration

4.4 Optimisation of parameter design based on energy balancing between passive components

4.4.1 Principle of energy balancing compensation between passive components

4.4.2 Parameter of passive components selection for simulation and prototype

4.4.3 Principle of conventional PFC SEPIC structure
4.5 Effect of unbalanced energy at the output of full-bridge

4.5.1 Elimination of dead zones based on input and output inductor currents in DCM and CCM 66

4.5.2 Elimination of extra energy at full-bridge output voltage 69

4.5.3 Experimental results of dead zones and extra energy elimination 70

4.6 Improvement of $THD_i$ 71

4.6.1 Simulation and experimental results of $THD_i$ improvement for SSBPFC SEPIC structure with SLDC configuration 72

4.7 Output voltage ripple reduction 76

4.7.1 Simulation and experimental results of output voltage ripple for SSBPFC SEPIC structure with SLDC configuration 76

4.8 Summary 79

CHAPTER 5 ELIMINATION OF CIRCULATING CURRENT AND UNDESIRED CAPACITIVE COUPLING LOOP 81

5.1 Overview 81

5.2 Principle of structure X, structure XI, and SSBPFC SEPIC structure with SLDC configuration 82

5.2.1 Structure X [54] 82

5.2.2 Structure XI 84

5.2.3 SSBPFC SEPIC structure with SLDC configuration 86

5.3 Features of SSBPFC SEPIC structure with SLDC configuration 88

5.4 Principle of elimination of circulating current and maximum current stress reduction at line-diodes 89
5.4.1 Simulation and experimental results of elimination of circulating current and reduction of maximum current stress at line-diodes 90

5.5 Effect of maximum current stress reduction at line-diodes 93

5.5.1 Simulation and experimental results of maximum current stress reduction at line-diodes D₁ and D₂ 93

5.6 Principle of capacitive coupling loop and maximum current stress reduction at input capacitor 95

5.6.1 Simulation and experimental results of maximum current stress reduction at input capacitor 96

5.7 Elimination of capacitive coupling loop at input capacitor 98

5.7.1 Simulation and experimental results of capacitive coupling loop elimination at input capacitor 99

5.8 Summary 101

CHAPTER 6 CONCLUSIONS AND RECOMMENDATIONS FOR FUTURE WORK 103

6.1 Overview 103

6.2 Research contribution 104

6.3 Conclusions 106

6.4 Recommendations for future work 108

REFERENCES 109

APPENDIX A 117

APPENDIX B 118

APPENDIX C 119

APPENDIX D 120

APPENDIX E 129
## LIST OF TABLES

<table>
<thead>
<tr>
<th></th>
<th>Description</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>2.1</td>
<td>Comparison between uncontrolled and controlled full wave rectifiers</td>
<td>15</td>
</tr>
<tr>
<td>2.2</td>
<td>Summary number of components in BPFC topologies</td>
<td>20</td>
</tr>
<tr>
<td>2.3</td>
<td>Limit for class D equipment with input power less than 600 W</td>
<td>24</td>
</tr>
<tr>
<td>3.1</td>
<td>Values of passive components for existing BPFC SEPIC structures</td>
<td>30</td>
</tr>
<tr>
<td>3.2</td>
<td>Summary of previous issues on BPFC SEPIC</td>
<td>42</td>
</tr>
<tr>
<td>3.3</td>
<td>Parameter design of passive components</td>
<td>49</td>
</tr>
<tr>
<td>3.4</td>
<td>Summary of improvement based on issues in BPFC SEPIC structures</td>
<td>52</td>
</tr>
<tr>
<td>4.1</td>
<td>Parameters setup for simulation and prototype</td>
<td>64</td>
</tr>
<tr>
<td>4.2</td>
<td>Parameters selection before and after optimisation of passive components</td>
<td>64</td>
</tr>
</tbody>
</table>
# LIST OF FIGURES

<table>
<thead>
<tr>
<th>Figure</th>
<th>Description</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.1</td>
<td>General research framework related to three objectives</td>
<td>6</td>
</tr>
<tr>
<td>2.1</td>
<td>Comparison of AC system, DC system of 48 V, and HVDC system [1]</td>
<td>10</td>
</tr>
<tr>
<td>2.2</td>
<td>AC and DC power distribution systems [1]</td>
<td>11</td>
</tr>
<tr>
<td>2.3</td>
<td>Power converters for Datacom and Telecom applications with battery backup system [9]</td>
<td>12</td>
</tr>
<tr>
<td>2.4</td>
<td>Power converters for Datacom and Telecom applications</td>
<td>13</td>
</tr>
<tr>
<td>2.5</td>
<td>Block diagram of integration of two power converters</td>
<td>14</td>
</tr>
<tr>
<td>2.6</td>
<td>Classifications of single phase full wave rectifier [43]</td>
<td>15</td>
</tr>
<tr>
<td>2.7</td>
<td>Classification of DC-DC converter</td>
<td>16</td>
</tr>
<tr>
<td>2.8</td>
<td>Conventional PFC SEPIC structure [43]</td>
<td>17</td>
</tr>
<tr>
<td>2.9</td>
<td>Block diagram of reduction in number of power converters</td>
<td>18</td>
</tr>
<tr>
<td>2.10</td>
<td>Classification of BPFC topologies [49]</td>
<td>19</td>
</tr>
<tr>
<td>2.11</td>
<td>Diode clamped BPFC with coupling inductor [50]</td>
<td>19</td>
</tr>
<tr>
<td>2.12</td>
<td>Switch clamped BPFC [51]</td>
<td>19</td>
</tr>
<tr>
<td>2.13</td>
<td>General classification of PFC circuit [52]</td>
<td>21</td>
</tr>
<tr>
<td>2.14</td>
<td>Power Factor [65] (a) Unity, (b) Lagging, and (c) Leading</td>
<td>25</td>
</tr>
<tr>
<td>2.15</td>
<td>Dead zones occur at the AC current source [67]</td>
<td>26</td>
</tr>
<tr>
<td>2.16</td>
<td>Different types of bridge integration structure (a) Full-bridge rectifier with SEPIC structure (b) Half-bridge rectifier with SEPIC structure</td>
<td>27</td>
</tr>
<tr>
<td>3.1</td>
<td>Flowchart for circuit structure simplification</td>
<td>29</td>
</tr>
<tr>
<td>3.2</td>
<td>Issues in separated-operation and shared-operation structures</td>
<td>31</td>
</tr>
<tr>
<td>3.3</td>
<td>SEPIC structure</td>
<td>32</td>
</tr>
<tr>
<td>3.4</td>
<td>Structure I [71]</td>
<td>33</td>
</tr>
<tr>
<td>3.5</td>
<td>Structure II (proposed structure to improve structure I)</td>
<td>33</td>
</tr>
<tr>
<td>3.6</td>
<td>Structure III (proposed structure to improve structure II)</td>
<td>34</td>
</tr>
</tbody>
</table>
3.7 Structure IV (proposed structure to improve structure III) 34
3.8 Structure V [60] 35
3.9 Structure VI (proposed structure to improve structure V) 36
3.10 Structure VII (proposed structure to improve structure VI) 36
3.11 Structure VIII [56] 37
3.12 Structure IX (proposed structure to improve structure VIII) 38
3.13 Structure X [54] 39
3.14 Structure XI (proposed structure to improve structure X) 39
3.15 SLDC as the proposed configuration 40
3.16 Structure XII (TSBPFCS EPIC with SLDC configuration) 41
3.17 Structure XIII (SSBPFCS EPIC with SLDC configuration) 41
3.18 Main theoretical waveforms for switching period 43
3.19 Large-signal circuit model of [32] and SSBPFCS EPIC structure with SLDC configuration 45
3.20 AC voltage source and THD, at different duty cycle values 49
3.21 Output voltage gain versus duty cycle 50
3.22 $D_{\text{effective}}$ versus RMS-voltage AC source with fixed DC voltage output of 48 V 51
3.23 Classification of BPFC SEPIC structures 53
4.1 Flowchart general process for power quality issues mitigation 55
4.2 Full-bridge diode rectifier 56
4.3 AC source and inconstant DC output voltage 56
4.4 SLDC configuration for BPFC structure 57
4.5 AC source and chopped DC output voltage 57
4.6 Voltage gain versus duty cycle based on SLDC configuration 58
4.7 Conventional PFC SEPIC structure 59
4.8 Conventional bridgeless SEPIC structure [58] 60
4.9 SSBPFCS EPIC structure with SLDC configuration 61
4.10 Principle of energy balancing compensation between passive components 63
4.11 Mode of operation for conventional PFC SEPIC structure (a) Mode-1, (b) Mode-2, (c) Mode-3, (d) Mode-4, (e) Mode-5, (f) Mode-6 65
4.12 Extra energy and dead zones elimination consideration based on conventional PFC SEPIC 66
4.13 Operation mode for input and output inductors for conventional PFC SEPIC structure (a) DCM and DCM (b) DCM and CCM, respectively 68

4.14 Operation mode for input and output inductors for SSBPFC SEPIC structure with SLDC configuration (a) DCM and DCM (b) DCM and CCM, respectively 68

4.15 Dead zones and no dead zones 69

4.16 Dead zones and high current ripple at AC current source 69

4.17 Full-bridge Output voltage, \( V_1 \) (a) Extra energy (b) Optimum energy in conventional PFC SEPIC structure 69

4.18 Quality of AC current source and full-bridge output voltage, \( V_1 \) (a) Extra energy (b) Optimum energy in conventional PFC SEPIC structure 71

4.19 Frequency spectrum of AC current source for the simulated SSBPFC SEPIC structure with SLDC configuration (a) Before optimisation (b) After optimisation 72

4.20 Waveform quality of AC current source (a) Before optimisation 74

4.21 Frequency spectrum of AC current source for SSBPFC SEPIC with SLDC configuration obtained experimentally (a) Before optimisation (b) After optimisation 74

4.22 Frequency spectrum for Structure X and improved proposed (SSBPFC SEPIC with SLDC configuration) structure (a) Before optimisation (b) After optimisation 75

4.23 Output ripple frequency for (a) Full-bridge rectifier (b) Half-bridge rectifier 77

4.24 Comparisons of output voltage and current ripples for simulated SSBPFC SEPIC structure with SLDC configuration (a) \( C_o = 470 \, \mu F \), (b) \( C_o = 3300 \, \mu F \) 77

4.25 Experimental results of output voltage ripple with different value of output capacitor (a) 470 \, \mu F (b) 3300 \, \mu F 79

4.26 Ripple balancing between input and output inductors current ripple 80

5.1 Modes of operation for structure X (a) Mode-1, Mode-2, and Mode-3, (b) Mode-7, Mode-8, and Mode-9, (c) Mode-4, Mode-5, and Mode-6, (d) Mode-10, Mode-11, and Mode-12 84
<table>
<thead>
<tr>
<th>Section</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>5.2</td>
<td>Modes of operation for structure XI (a) Mode-1 and Mode-2, (b) Mode-6 and Mode-7, (c) Mode-3 and Mode-4, (d) Mode-8 and Mode-9, (e) Mode-5, (f) Mode-10</td>
</tr>
<tr>
<td>5.3</td>
<td>Modes of operation for SSBPFC SEPIC structure with SLDC configuration (a) Mode-1 and Mode-2, (b) Mode-5 and Mode-6, (c) Mode-3 and Mode-4, (d) Mode-7 and Mode-8</td>
</tr>
<tr>
<td>5.4</td>
<td>Different position of diodes based on (a) Structure X (b) SSBPFC SEPIC structure with SLDC configuration</td>
</tr>
<tr>
<td>5.5</td>
<td>Current at input inductor, $L_1$ for structure X and SSBPFC SEPIC structure with SLDC configuration obtained from simulation</td>
</tr>
<tr>
<td>5.6</td>
<td>Current at input inductor, $L_1$ (a) Circulating current for structure X</td>
</tr>
<tr>
<td>5.7</td>
<td>Maximum current stress at diodes based on (a) Structure X</td>
</tr>
<tr>
<td>5.8</td>
<td>Simulation result for maximum current stress reduction at line-diodes based on structure X and SSBPFC SEPIC structure with SLDC configuration</td>
</tr>
<tr>
<td>5.9</td>
<td>Maximum current stress at line-diode, $D_1$ for (a) Structure X (b) SSBPFC SEPIC structure with SLDC configuration for experiment</td>
</tr>
<tr>
<td>5.10</td>
<td>Circulating current and looping current path between input capacitors based on (a) Structure X (b) Structure XI</td>
</tr>
<tr>
<td>5.11</td>
<td>Different current stress at the input capacitors based on structure X and structure XI obtained from simulation</td>
</tr>
<tr>
<td>5.12</td>
<td>Maximum current stress reduction at input capacitor (a) Structure X (b) Structure XI obtained from experiment</td>
</tr>
<tr>
<td>5.13</td>
<td>Reduction in number of input capacitors for elimination of capacitive coupling loop (a) Structure XI (b) SSBPFC SEPIC structure with SLDC configuration</td>
</tr>
<tr>
<td>5.14</td>
<td>Elimination of capacitive coupling loop at the input capacitor by reducing number of the capacitor obtained from simulation</td>
</tr>
<tr>
<td>5.15</td>
<td>Maximum current stress reduction at input capacitor (a) Structure XI and (b) SSBPFC SEPIC structure with SLDC configuration obtained from experiment</td>
</tr>
<tr>
<td>6.1</td>
<td>SLDC as the proposed configuration</td>
</tr>
<tr>
<td>6.2</td>
<td>Principle of energy balancing compensation between passive components</td>
</tr>
</tbody>
</table>
6.3 SSBPFC SEPIC structure
LIST OF SYMBOLS AND ABBREVIATIONS

$f_{line}$ - Line Frequency
$f_r$ - Resonant Frequency
$f_{sw}$ - Switching Frequency
$PF$ - Power Factor
$THD_i$ - Total Harmonic Distortion of AC current source
AC - Alternating Current
BPFC - Bridgeless Power Factor Correction
CCM - Continuous-Conduction Mode
Datacom - Data Communication
DC - Direct Current
DCM - Discontinuous-Conduction Mode
EMI - Electromagnetic Interference
ESR - Equivalent Series Resistor
ETSI - European Telecommunications Standards Institute
FPGA - Field-Programmable Gate Array
ICT - Information And Communications Technology
IGBT - Insulated-Gate Bipolar Transistor
MOSFET - Metal Oxide Semiconductor Field Effect
NTT - Nippon Telegraph And Telephone Corporation
PFC - Power Factor Correction
PLECS - Piecewise Linear Electrical Circuit Simulation
PWM - Pulse Width Modulation
SEPIC - Single-Ended Primary-Inductor Converter
SLDC - Series-Line-Diode-clamped
SSBPFC - Single-Switch Bridgeless Power Factor Correction
TSBPFC - Two-Switch Bridgeless Power Factor Correction
<table>
<thead>
<tr>
<th>Abbreviation</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Telecom</td>
<td>Telecommunications</td>
</tr>
<tr>
<td>THD</td>
<td>Total Harmonic Distortion</td>
</tr>
<tr>
<td>TSBPFC</td>
<td>Two-Switch Bridgeless Power Factor Correction</td>
</tr>
<tr>
<td>UTHM</td>
<td>Universiti Tun Hussein Onn Malaysia</td>
</tr>
<tr>
<td>UPS</td>
<td>Uninterruptible Power Supply</td>
</tr>
</tbody>
</table>
**LIST OF APPENDICES**

<table>
<thead>
<tr>
<th>APPENDIX</th>
<th>TITLE</th>
<th>PAGE</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>NTT Activity</td>
<td>117</td>
</tr>
<tr>
<td>B</td>
<td>Harmonic Order Following IEC 61000-3-2 Standards</td>
<td>118</td>
</tr>
<tr>
<td>C</td>
<td>Overview: Improvement of BPFC SEPIC structures to reduce number of passive components</td>
<td>119</td>
</tr>
<tr>
<td>D</td>
<td>ABC200 Series AC-DC Open Frame Power Supplies</td>
<td>120</td>
</tr>
<tr>
<td>E</td>
<td>Parameter Design for Passive Components</td>
<td>129</td>
</tr>
<tr>
<td>F</td>
<td>Overview: Optimisation of passive components parameters to mitigate power quality issues</td>
<td>132</td>
</tr>
<tr>
<td>G</td>
<td>Specification of Components</td>
<td>133</td>
</tr>
<tr>
<td>H</td>
<td>FPGA Block Diagram</td>
<td>149</td>
</tr>
<tr>
<td>I</td>
<td>Experimental Setup</td>
<td>150</td>
</tr>
<tr>
<td>J</td>
<td>Hardware Circuit Structure</td>
<td>153</td>
</tr>
<tr>
<td>K</td>
<td>Overview: Elimination of circulating current and undesired capacitive coupling loop</td>
<td>154</td>
</tr>
</tbody>
</table>
CHAPTER 1

INTRODUCTION

1.1 Project background

Computer network or data network has become a necessity in industries, education fields, and societies. This growth has been driven by an increasingly connected worldwide population. Therefore, the information and communications technology (ICT) plays a main part to provide the data network and networking connection. The ICT refers to the technologies that provide access to information through telecommunications. The ICT equipment is required to realize the development of ICT. The Data Communication (Datacom) processes and stores the data of information transferred from the sender to the receiver, and Telecommunications (Telecom) sends the information over distances [1]–[3]. In recent years, the ICT equipment in Datacom application is commonly located in the same room, cabinet or rack like the conventional telecom equipment [4]. The Datacom application requires a DC source of +48 V and uses uninterruptible power supply (UPS) as the backup supply [5]–[21]. The desired voltage for the Datacom application follows the universal standard for telecommunications equipment that is clearly defined by European Telecommunications Standards Institute (ETSI) [22]. Most of the ICT equipment require input supply in direct current (DC) but, the available sources are mainly in alternating current (AC) system.

The Nippon Telegraph and Telephone Corporation (NTT) [23] has proposed three systems for the Datacom application namely the AC system, DC system with 48 V, and HVDC system with 400 V [1]. The DC system with 48V is currently used worldwide as the system has less number of power converter, simple configuration,
high reliability, and low cost compared to the AC system. The power converter plays an important role to ensure the ICT equipment in Datacom application can receive the DC source fixed in 48 V following the standard of ICT equipment [24]. Thus, the application needs an AC-DC converter (full-bridge rectifier) to convert the AC source from the grid to DC output. The AC-DC converters consist of diodes or thyristors to provide a controlled and uncontrolled DC power with unidirectional and bidirectional power flows [25]. When a single phase full-bridge rectifier is connected to non-linear load such as the ICT equipment, it results in poor power quality such as voltage distortion, low power factor (PF) at the AC sources, high total harmonics distortion of current (THD), and slowly varying rippled DC output at the end load [26]. Accordingly, a single-ended primary-inductor converter (SEPIC) is selected to improve the PF, reduce THD, and output voltage ripple as well as stepping down the voltage to 48 V [27]–[29]. Integration of two converters which are the full bridge rectifier and SEPIC converter is named as conventional PFC SEPIC. When the conventional PFC SEPIC is implemented in the DC system of 48 V, the structure has several integration issues such as common mode noise and high conduction loss due to the four diodes-bridge deployed. Therefore, mitigation solutions are needed to avoid the ICT equipment and their connection into the grid from damage.

Back in 1983, the first bridgeless PFC (BPFC) topology is proposed by D. M. Mitchel [30] to reduce the conduction loss as well as to reduce the number of power converter [31]. The BPFC topology means that two operation circuits operate in one circuit. It is good to know that a single-stage BPFC uses one DC-DC converter while the two-stage BPFC uses two DC-DC converters in the topology. Usually, the BPFC boost converters are widely used in other applications due to its less number of passive components, has simple configuration, low cost, and robust [32]–[34]. But the BPFC boost is not suitable to be used in the DC system with 48 V due to the DC output of the BPFC boost is higher than the AC source. The BPFC boost structure possesses some disadvantages in which the DC output isolation is hard to be implemented, high start-up inrush current, and the current limitation is low during overload conditions [32], [35]–[39]. Therefore, the BPFC SEPIC in [32] is proposed to solve the disadvantages of the previous BPFC boost converter as well as able to follow the standard of the ICT equipment. However, the BPFC SEPIC has other major practical drawbacks such as more number of components, using two switches, circulating current, capacitive coupling loop, and maximum current stress at the semiconductor
and passive components. Thus, the structure needs improvement and optimisation of the parameter of components.

To solve the major practical drawbacks of the existing BPFC SEPIC, this research is focusing on the circuit structure simplification and power quality issues mitigation. The circuit simplification is from the improvement of circuit structure, and the power quality issues mitigation is based on the optimisation of parameter design. The improvement of the circuit structure is required to ensure the number of components can be reduced, $PF$ can achieve nearly unity, and the configuration is simple. From the structure design, an approximately unity $PF$ can also be achieved by rearranging the position of the clamped diodes while optimising the parameter design. Hence, an improved configuration for the BPFC SEPIC which is the series-line-diode-clamped (SLDC) configuration is introduced. The design of the bridgeless PFC (BPFC) SEPIC structure with SLDC configuration aims to eliminate the circulating current and capacitive coupling loop, causing the maximum current stress at the semiconductor and passive component to be reduced as well. To mitigate the power quality issues in the structure, the principle of energy balancing between passive components, ripple balancing concept, and large capacitance of output capacitance are used for the purpose to optimising parameter design. When the parameter of the passive components are optimised, the results show that the structure produces a low $THD$, and good waveform quality of AC sources without presence of dead zones, reduced output voltage ripple, and almost unity $PF$.

1.2 Problem statements

The most popular available source worldwide is AC source while majority of devices or applications such as ICT equipment in Datacom application require DC 48 V as the input DC. A conventional PFC SEPIC structure is presented to produce a fixed DC voltage output of 48 V for Datacom application but suffers from integration issues. Thus, BPFC SEPIC with separated-operation is introduced to solve the integration issues in conventional PFC SEPIC but the structure requires more number of components. Therefore, the BPFC SEPIC with shared-operation structure is presented to reduce the number of components, however, it possesses some major practical drawbacks which are circulating current losses, capacitive coupling loop, and
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